

LONWORKS[®]

Twisted Pair Control Module

User's Guide

Version 2



E C H E L O N[®]

Corporation



078-0015-01E

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Document No. 59100

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Chapter 1

Introduction

Echelon's LONWORKS Twisted Pair Control Modules contain the core elements for OEM node designs using LONWORKS technology. The core elements of a control module are a Neuron[®] 3150[®] Chip, crystal clock circuit, JEDEC MO-052 AE PLCC memory socket (32-pin rectangular), twisted pair transceiver, and unbuffered access to the Neuron Chip I/O, ~SERVICE, and ~RESET signals.

The family of six LONWORKS Twisted Pair Control Modules shares a common footprint and I/O interface to allow systems with different media requirements to share common application electronics board designs. The available modules include:

Module	Features
TP/FT-10 Free Topology Control Module	Transformer-isolated, free topology, 78kbps, 5MHz clock
TP/FT-10F Free Topology Flash Control Module	Transformer-isolated, free topology, 78kbps, flash memory support, 10MHz clock
TP/XF-78 Control Module	Transformer-isolated, bus operation, 78kbps, 5MHz clock
TP/XF-78F Flash Control Module	Transformer-isolated, bus operation, 78kbps, flash memory support, 10MHz clock
TP/XF-1250 Control Module	Transformer-isolated, bus operation, 1.25Mbps, 10MHz clock
TP-RS485 Control Module	RS-485, bus topology, variable bit rate, 5MHz clock

Audience

The *LONWORKS Twisted Pair Control Module User's Guide* provides specifications and user instruction for customers who have purchased any of Echelon's Twisted Pair Control Modules.

Content

This manual provides detailed technical specifications on the electrical and mechanical interfaces and operating environment characteristics for the control modules.

This document also provides guidelines for migrating applications from a LonBuilder[®] Neuron Emulator to a control module-based product design. References and vendor sources are included to simplify the task of integrating the control modules with application electronics.

This document has a list of references in Chapter 8. Whenever a reference document is addressed, a superscript number corresponding to the reference has been placed in the text, i.e., Standler⁹. Whenever a specific chapter or section within a reference has been referred to, the reference is enclosed in brackets and the chapter is addressed by number, i.e., Reference [1], Chapter 8.

Related Documentation

The following Echelon documents are suggested reading:

LonBuilder User's Guide (078-0001-01)

Neuron C Programmer's Guide (078-0002-01)

Neuron C Reference Guide (078-0140-01)

NodeBuilder User's Guide (078-0141-01)

LonBuilder Hardware Guide (078-0003-01)

LONMARK Layers 1-6 Interoperability Guidelines (078-0014-01)

LONMARK Application Layer Interoperability Guidelines (078-0120-01)

Neuron Chip Data Book as published by Motorola and Toshiba

Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks (005-0023-01)

LONWORKS Custom Node Development (005-0024-01)

LONWORKS TPT Twisted Pair Transceiver Module User's Guide (078-0025-01)

LONWORKS FTT-10 Free Topology Transceiver User's Guide (078-0114-01)

LONWORKS FTT-10A Free Topology Transceiver User's Guide (078-0156-01)

LONWORKS LPT-10 Link Power Transceiver User's Guide (078-0105-01)

LONWORKS LPI-10 Link Power Interface Module User's Guide (078-0104-01)

Chapter 2

Electrical Interface

Twisted Pair Control Modules interface to the node application electronics and to the network through two connectors, P1 and P2, respectively. P1 provides access to the Neuron Chip I/O, \sim RESET, and \sim SERVICE pins, and the power connection for the control module (see Chapter 4 for power supply requirements). P2 supports connection to the twisted pair data network, and for the TP/XF control modules, P2 also provides access to the network coupling transformer.

P1 and P2 Connector Terminals

The pinout of the P1 and P2 connector terminals is shown in tables 1, 2, and 3. The I/O pin function names defined in table 1 are identical to the terms used in the *Neuron Chip Data Book*¹ which defines the functions and electrical characteristics for those signal names listed in table 1. The I/O signals are connected directly to the Neuron 3150 Chip without buffering.

Table 1 18-pin I/O Connector (P1) for Control Modules

Name	Pin #	Function
IO0	2	***
IO1	4	
IO2	6	
IO3	8	
IO4	10	
IO5	11	
IO6	13	
IO7	15	
IO8	17	
IO9	14	
IO10	16	
~RESET	9	
~SERVICE	18	
+5V	12	power supply input
GND	3, 5, 7	power supply ground
	1	no connection

Table 2 6-pin Network Connector (P2) for the TP/XF Control Modules

Name	Pin #	Function
CTB	1	transformer center tap **
CTA	2	transformer center tap **
Data B	3	network data B signal
Data A	4	network data A signal
	5	no connection
	6	no connection

Table 3 6-pin Network Connector (P2) for the TP/FT-10, TP/FT-10F, and TP-RS485 Control Modules ****

Name	Pin #	Function
	1	no connection
	2	no connection
Data B	3	network data B signal *
Data A	4	network data A signal *
	5	no connection
	6	no connection

* The TP/FT-10 and TP/FT-10F Control Modules incorporate DC blocking capacitors and therefore can directly connect to either non-link power or link power channels.

** CTA and CTB must be shorted together on the applications electronics board.

*** See the *Neuron Chip Data Book*¹ for the pin definition of the Neuron Chip's I/O and 5-pin communications ports.

**** Refer to the *EIA RS-485 Standard*¹⁴ Electronic Industries Association, 1983 for information on ground referencing RS-485-based devices and cable shield wires.

Control Module pin P1.9 is the Neuron Chip \sim RESET pin. The \sim RESET pin on the Neuron Chip may be driven externally or may be used as an open drain output to provide a reset signal for the application circuit. The details of the recommended circuit and loading on the Neuron Chip \sim RESET pin are described in Reference [1].

The inherent loading on the \sim RESET pin for the Control Modules is shown in table 4. The TP/XF-78F, TP/FT-10, and TP/FT-10F Control Modules include an on-board low voltage indicator (LVI).

Table 4 Control Module \sim RESET Characteristics

Control Module	\simRESET Loading	External LVI
TP/FT-10	136pF	Included on module
TP/FT-10F	136pF	Included on module
TP/XF-78	136pF	Required on motherboard
TP/XF-78F	136pF	Included on module
TP/XF-1250	136pF	Required on motherboard
TP-RS485	136pF	Required on motherboard

The \sim SERVICE pin of the Neuron Chip is accessible directly at P1.18. This pin is used for various network installation and maintenance scenarios. The function of this pin is described in Reference [1]. By default, the internal pull-up resistor for the \sim SERVICE pin is enabled. Typical applications will use the circuit shown in figure 1. The internal pull-up may be disabled using a compiler directive `#pragma disable_servpin_pullup` in the application code targeted for the node.

Typical applications do not require debounce conditioning of momentary push buttons attached to the \sim SERVICE and \sim RESET pins. The software response time associated with these inputs is long enough to effectively provide a software debounce for switches with a contact bounce settling time as long as 20 msec.

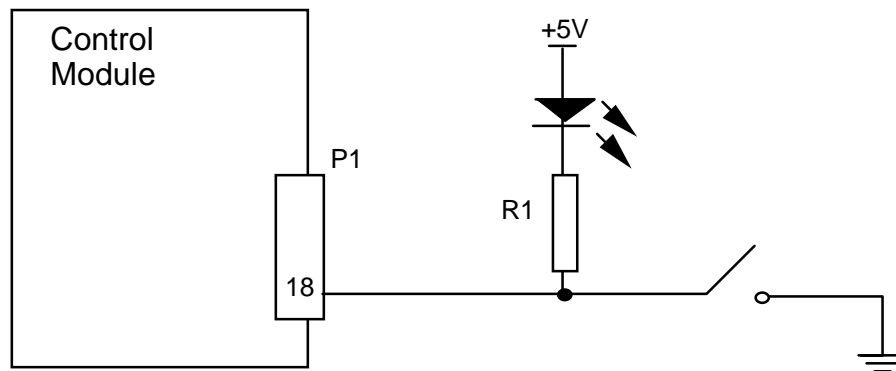


Figure 1 Typical \sim SERVICE Pin Circuit

Chapter 3

Mechanical Considerations

This chapter discusses the mechanical footprint and connectors of the Twisted Pair Control Modules. Details of mounting to an application electronics board are provided.

Mechanical Footprint

The Twisted Pair Control Modules share a common footprint and connectors as shown in figure 2. The most common control module mounting scenario uses socket strips on the application electronics board which connect with P1 and P2 as shown in figure 3. Vendor information for socket strips that mate with the 0.025" (0.64mm) square header posts of P1 and P2 are referenced in table 5.

If necessary, taller socket strips may be used to gain more clearance between the control module and the application board. Decisions about component placement on the application electronics board must also consider electromagnetic interference (EMI) and electrostatic discharge (ESD) issues discussed in Chapter 6 of this document.

Figures 3A and 3B show the maximum height of parts on both sides of the control modules. Application designs using the transformer-isolated twisted pair transceivers should maintain a minimum of 0.15" (3.81mm) clearance from P2 pins and traces on the network side of the transformer to achieve the minimum isolation specified for these modules. Refer to the High Voltage and EMI Keepout sections in Chapter 6 for isolation requirements.

Three plated mounting holes that accept No. 6 (3.5mm) mounting screws are electrically connected to the control module ground plane. When the 0.025" (0.64mm) square posts of P1 and P2 are inserted into the sockets they provide enough holding strength (3 oz (85g)/pin) to secure the control module against shock and vibration to the operating limits of the components on the control module. However, at least one metal standoff and fastening screw located at the mounting hole near the P2 connector is recommended to meet EMI limits and for ESD protection (see Chapter 6).

For the TP/FT-10 control modules, the recommended metal standoff height is 0.56" (14.3mm) to provide adequate clearance. Note that the Methode Socket (referenced in table 3.1) in this case is not recommended, since its minimum insertion depth requirement is not met. Use of metal 0.50" (12.7mm) #6 standoffs together with metal spacers can achieve this. Alternately, metal 0.56" (14.3mm) #6 standoffs alone will be adequate. For the TP/XF, TP/FT-10F, and TP-RS485 control modules, 0.50" (12.7mm) #6 metal standoffs alone are recommended.

Figure 4 presents the height restrictions of the component side of the control module. The board is divided into two height zones: the maximum height of components in the first zone is 0.20" (5.1mm). The second zone's components are 0.47" (11.93mm) for the TP/XF and TP/FT-10F control modules and 0.555" (14.1mm) for the TP/FT-10 control module. Care should be taken to ensure that no components on the application electronics board interfere with the height restricted areas of the control modules.

Figure 5 shows the recommended PCB pad layout for the application electronics board to interconnect a control module with an application board that has socket strips mounted on the component side.

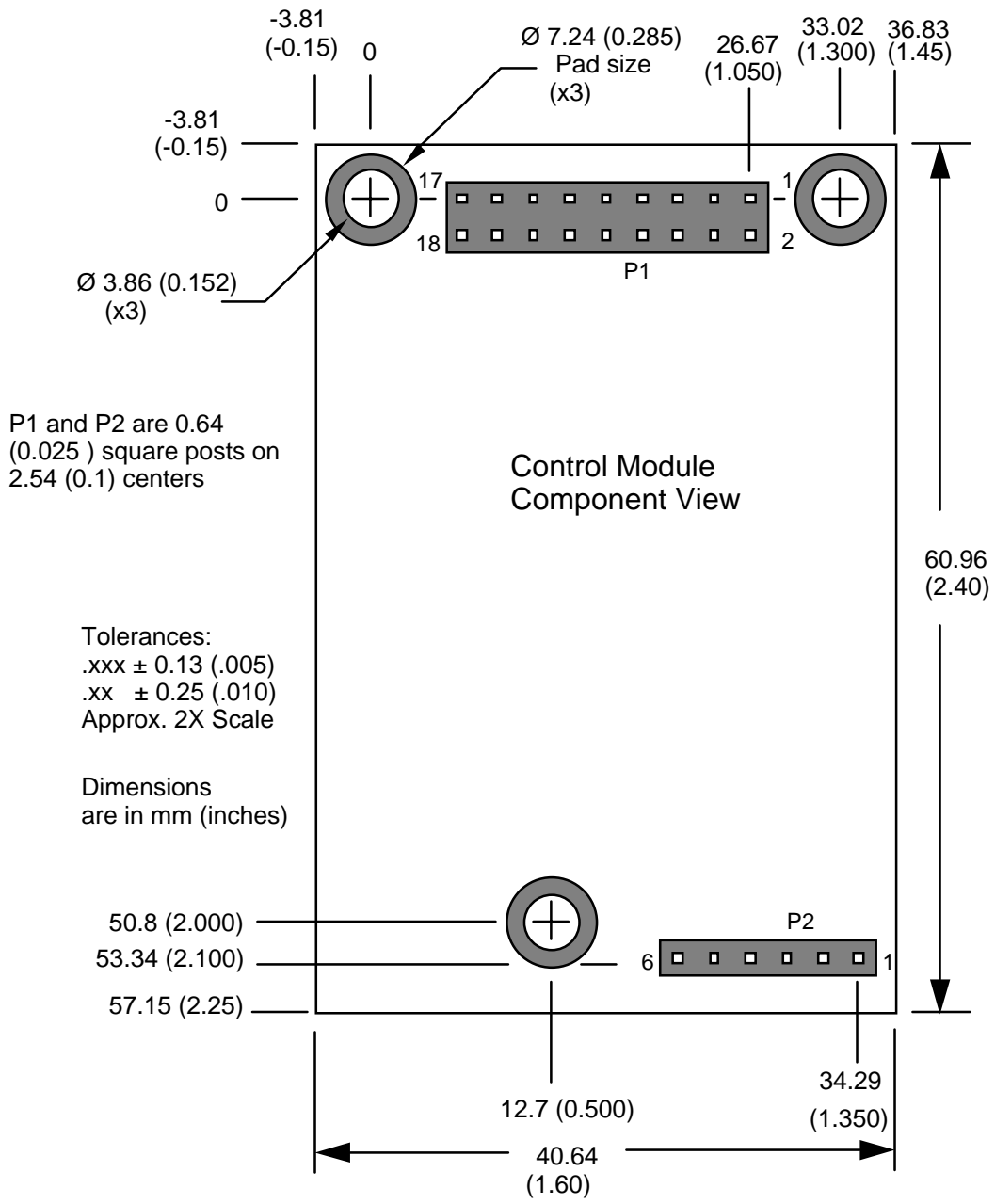


Figure 2 Control Module Mechanical Footprint

Table 5 Socket Strips Suitable for Use with the Control Module Header Pins

Manufacturer	P1: 18-pin (2 X 9)	P2: 6-pin (1 X 6)
Samtec	SSW-109-01-T-D	SSW-106-01-T-S
Methode *	9000-209-303	9000-106-303
Advanced Interconnections	BC-009-124TL	BC006-123TL

* Not recommended for use with the TP/FT-10 or TP/FT-10F Control Modules.

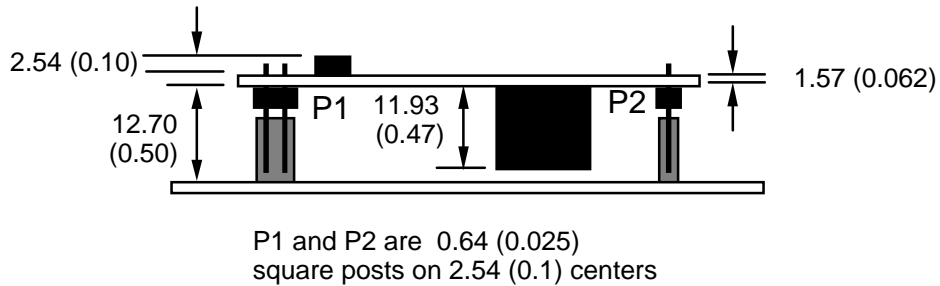


Figure 3A Recommended Spacing between the TP/XF-78, TP/XF-78F, TP/XF-1250, and TP-RS485 Control Modules and the Application Electronics Board

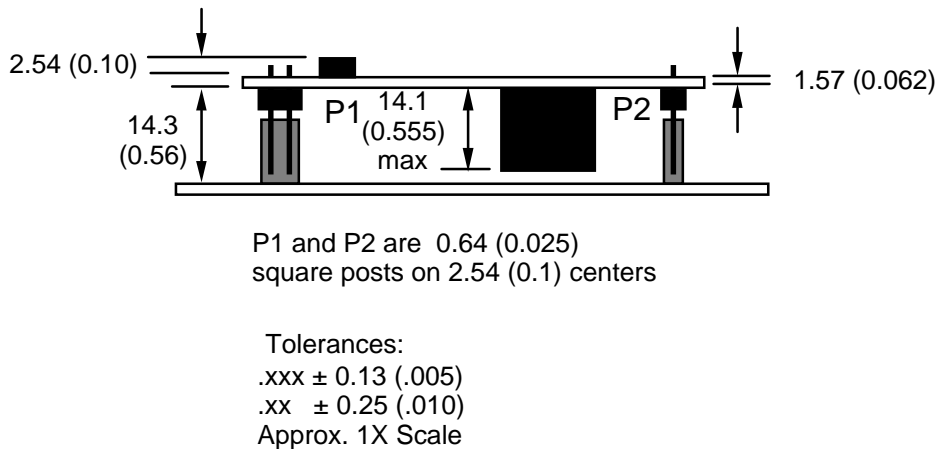


Figure 3B Recommended Spacing between the TP/FT-10 and TP/FT-10F Control Modules and the Application Electronics Board

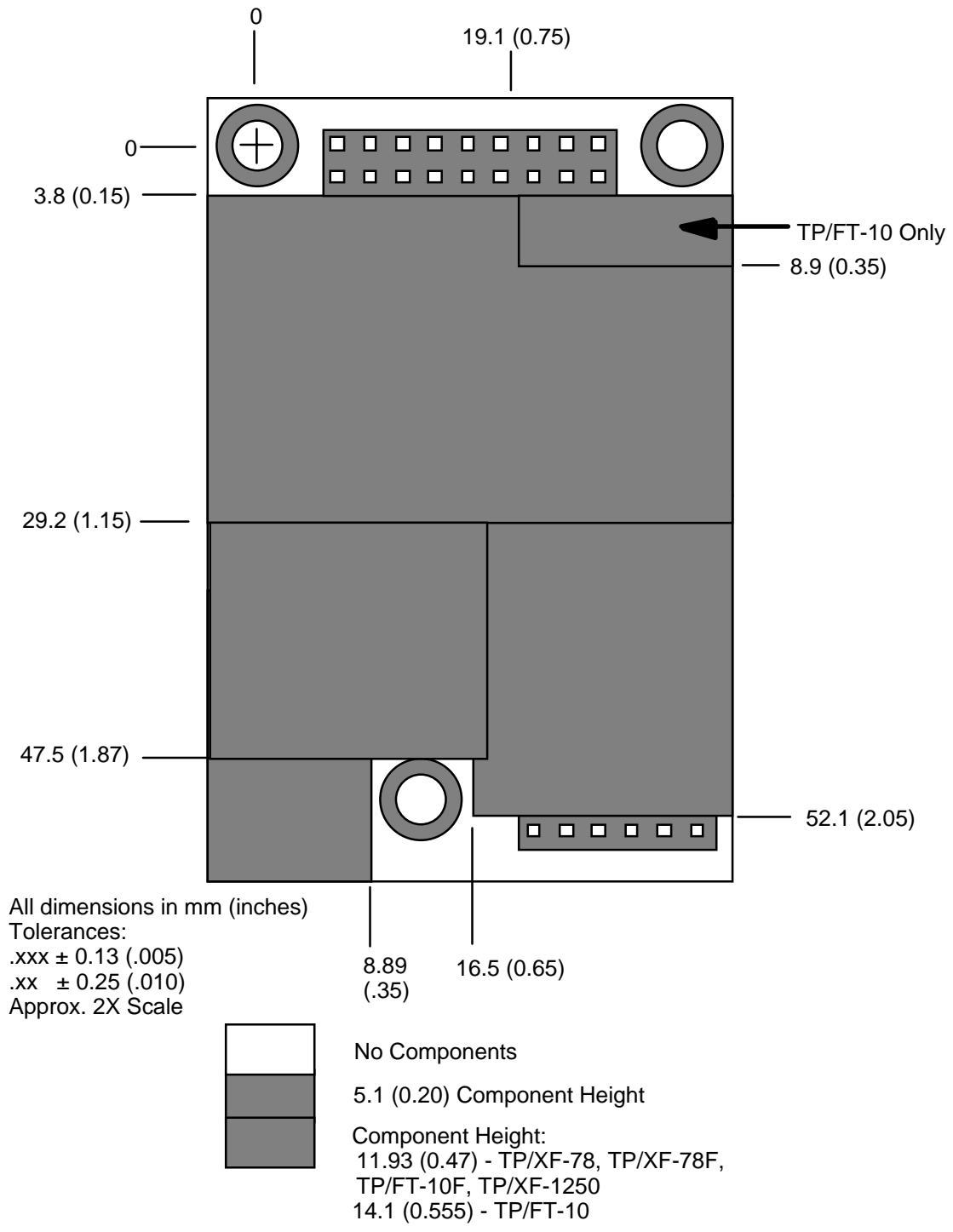


Figure 4 Vertical Component Profile for the Control Modules

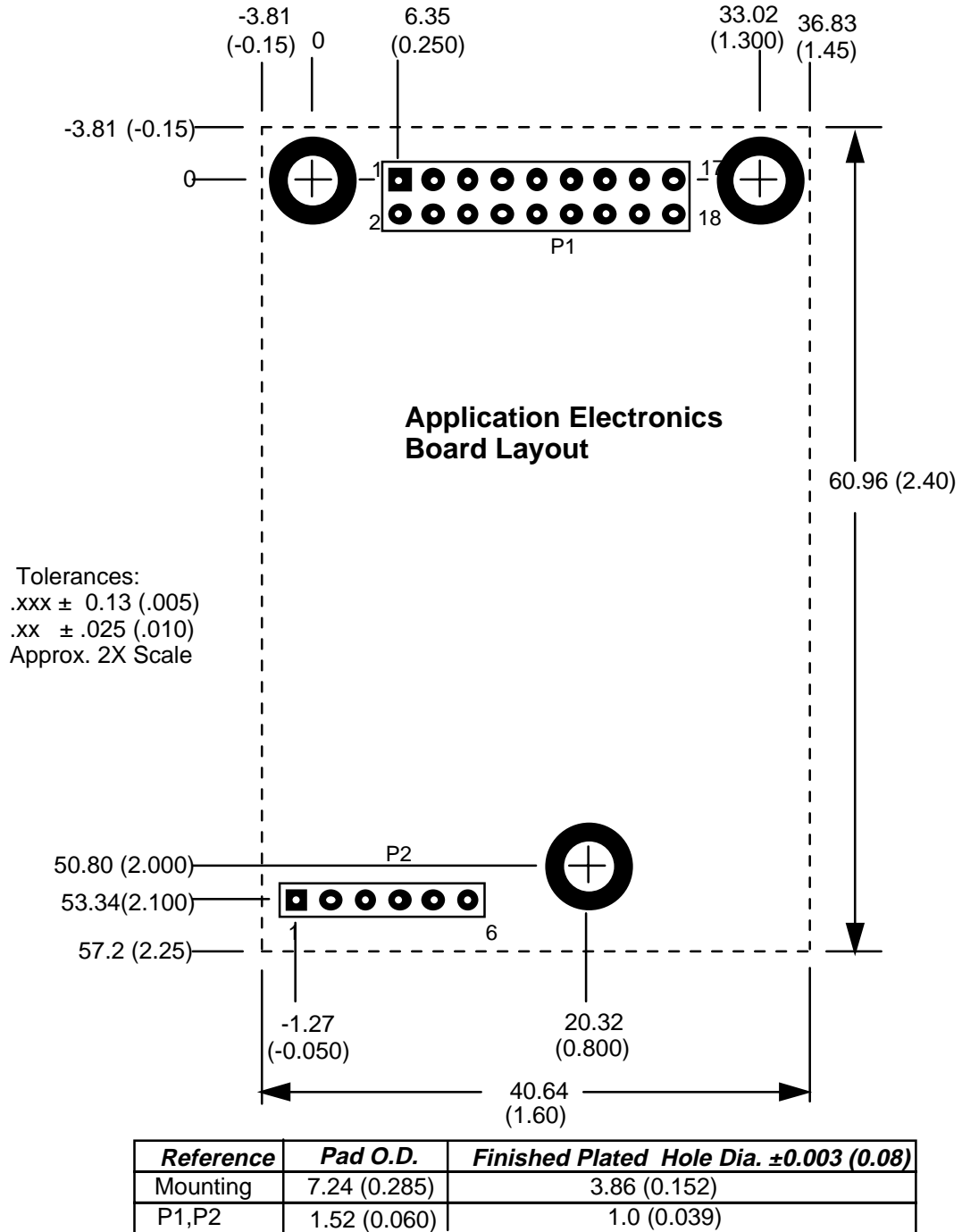


Figure 5 Required Pad Layout for Application Electronics Board

Chapter 4

Power Requirements

This section describes the power requirements for the control modules as well as considerations for noise filtering in order to comply with both conducted and radiated emissions requirements.

Control Module Power Requirements

Twisted Pair Control Modules require a +5VDC power source with sufficient current to power the control module in all modes of operation.

The supply current requirements for the control modules are outlined in table 6, which includes peak requirements for the different operating states of the Neuron Chip. The control modules require a 5V \pm 5% power supply. The current requirements are characterized for maximum number of nodes on the channel with I/O pins programmed as outputs at a logic low level with no load.

The values in table 6 are subject to change. Please consult current data sheets for the latest information.

Table 6 Typical Control Module +5 Volt Current Requirements

<i>Control Module</i>	<i>Typical DC Characteristics (+5.0V)</i>	
	Active, Receive (mA)	Active, Transmit (mA)
TP/FT-10 (5 MHz)	25	40
TP/FT-10F (10 MHz)	50	60
TP/XF-78 (5 MHz)	35	45
TP/XF-78F (10 MHz)	50	60
TP/XF-1250 (10 MHz)	55	80
TP-RS485 (5 MHz)	30	65

Notes:

1. Assumes internal I/O pullups are disabled and I/O lines are not connected to a load.
2. Assumes ~SERVICE pullup is enabled.
3. Includes CMOS EPROM running typical application with system code.
4. These figures include typical PROM current consumption of 4mA at 5MHz or 5mA at 10MHz; the TP/FT-10F and TP/XF-78F figures include flash memory reads, however, **flash memory writes require an additional 50mA**. These figures exclude current due to loading on the I/O connector pins.

Power Supply Decoupling and Filtering

The design of the control module power supply must consider the filtering and decoupling requirements of the control module. The power supply filter must prevent noise generated by the control module and I/O circuit from conducting onto external wires, and in the case of DC-DC switching power supplies, must prevent noise generated by the supply from interfering with module operation. Switching power supply designs must also consider the effects of radiated EMI.

The control modules include 2.2 μ F and 0.1 μ F power supply bypass capacitors close to pin 12 of P1. In general, a high frequency decoupling capacitor valued at 0.1 μ F or 0.01 μ F placed near pin 12 of P1 on the application electronics board is necessary to reduce EMI.

The control modules require a clean power supply to prevent RF noise from conducting onto the network through active drive circuits. Power supply noise near the network transmission frequency may degrade network performance.

Attention to the design of the application electronics circuit is also necessary. High speed signals and inductive loads are common sources of noise which must be managed by separating the logic and I/O power supplies, or by using sufficient filtering and decoupling techniques.

Chapter 5

Network Cabling and Connection

This chapter addresses cabling and termination for the TP/FT-10, TP/FT-10F, TP/XF-78, TP/XF-78F, and TP/XF-1250 Twisted Pair Control Modules. Included is an excerpt from the RS-485 Standard concerning grounding issues.

Performance Characteristics and Cabling

For TP/XF-78, TP/XF-78F, TP/XF-1250, and TP-RS485 performance characteristics and cabling information, refer to the sources of information shown in summary table 7. The specifications shown in table 7 are provided for convenience only and are not intended to be comprehensive.

Table 7 Module performance summary

Module	Cable Distance	Number of Nodes	Information Source
TP/FT-10, TP/FT-10F	Bus: 2700m (8850 feet) worst case with Belden 85102 cable Free topology: 500m (1640 feet) worst case with Belden 85102 cable	64 at -40 to +85°C	<i>FTT-10 User's Guide</i> (078-0114-01), <i>FTT-10A User's Guide</i> (078-0156-01), <i>LPT-10 User's Guide</i> (078-0105-01), Control Module Data Sheet 003-0121-01
TP/XF-78, TP/XF-78F	Bus: 1400m (4600 feet) worst case with 3m (10 feet) stubs with 22AWG (0.65mm) Level IV Cable	64 at 0 to +70°C	TPT User's Guide (078-0025-01), Control Module Data Sheet 003-0121-01
TP/XF-1250	Bus: 130m (430 feet) worst case with 0.3m (1 foot) stubs with 22AWG (0.65mm) Level IV Cable	64 at 0 to +70°C	Control Module Data Sheet 003-0121-01
TP-RS485 (39 kbps)	Bus: 1200m (3935 feet) with no stubs with 22AWG (0.65mm) Level IV Cable	32 at 0 to +70°C	Reference [14], Control Module Data Sheet 003-0121-01

Notes:

1. Worst case distance figures are based on variations in node distribution, node temperature, node voltage, wire characteristics, and Neuron Chip characteristics, and allow for an average wire temperature of up to +55°C.
2. Network length for TP/FT-10 channel varies by wire type.

Wire Characteristics - TP/FT-10 and TP/FT-10F

Due to the many cabling and termination options available for the TP/FT-10 channel, please refer to the *FTT-10 Free Topology Transceiver User's Guide* or *FTT-10A Free Topology Transceiver User's Guide*, as applicable, for information on wire characteristics and terminations.

Cable Terminations – Free Topology TP/FT-10 and TP/FT-10F

In a TP/FT-10 free topology segment, only one termination is required and may be placed anywhere on the free topology segment. There are two choices for the termination:

1. RC network (figure 6), with $R1 = 52.3 \text{ Ohms}$
2. LPI-10 Link Power Interface, with jumper at "1 CPLR" setting.

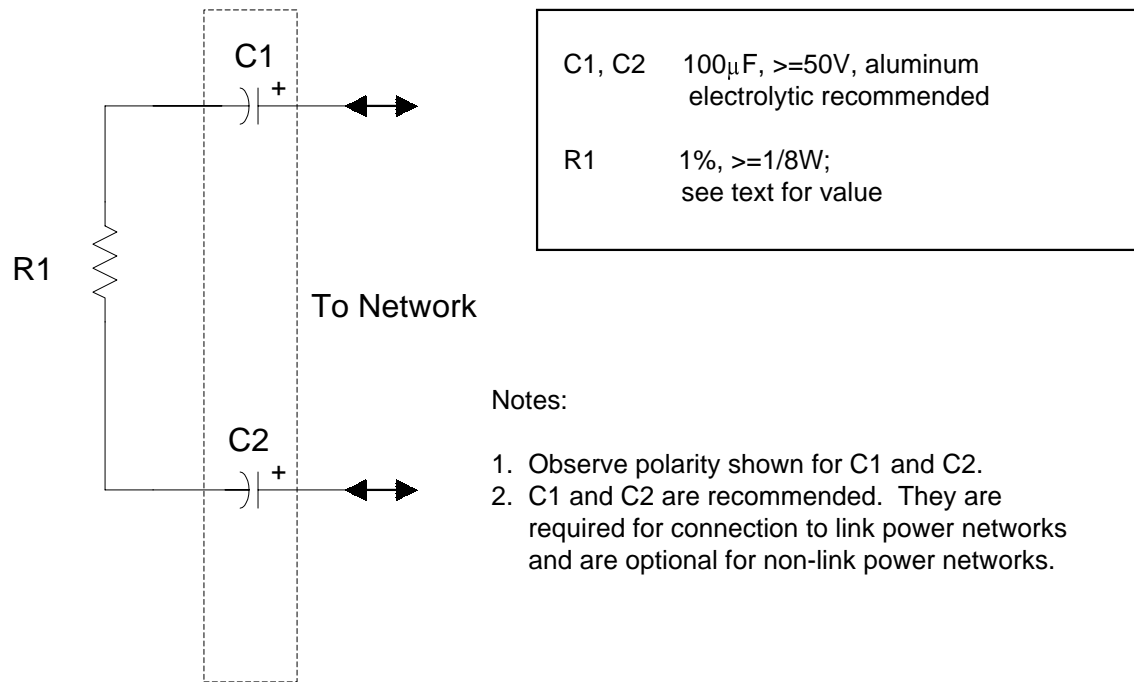


Figure 6 RC Network Termination for TP/FT-10 Segments

Cable Terminations – Doubly Terminated Bus Topology TP/FT-10 and TP/FT-10F

In a TP/FT-10 doubly terminated bus topology, two terminations are required, one at each end of the bus. There are two choices for each termination:

1. RC network (figure 6), with $R1 = 105$ Ohms.
2. LPI-10 Link Power Interface, with jumper at "2 CPLR" setting if resident on a link power segment. At this time, only one LPI-10 Interface is supported per segment, so at least one of the terminations must be the RC-type.

Wire Characteristics - TP/XF-78, TP/XF-78F, TP/XF-1250, and TP-RS485

The TP/XF-78, TP/XF-78F, TP/XF-1250, and TP-RS485 control modules are designed for distributed control applications using low-cost, Level IV twisted pair wire. The characteristics of the wire used to implement a network will affect the overall system performance with respect to total distance, stub length, and total number of nodes supported on a single channel. The control modules have been qualified using **only** Level IV, 22 AWG (0.65mm) twisted pair cable for the primary bus, and either Level IV, 24AWG (0.5mm) or Level IV, 22AWG cable for stubs where stubs are permitted. Under no circumstances should smaller gauge Level IV cable be substituted for Level IV, 22 AWG (0.65mm) twisted pair cable for the bus, or should Category IV cable be used in lieu of Level IV cable. Echelon periodically qualifies new cables for twisted pair transceivers, and it is advisable to check with Echelon from time to time to determine if new cables are available for use with the control modules.

The characteristics and suppliers of Level IV cable are described in the document *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks* ¹³ (Echelon part 005-0023-01).

Node Distribution Rule for TP/XF-1250 Segments

Due to the transmission characteristics of the TP/XF-1250 channel, communication failures may result from reflections of the TP/XF-1250 module's 1.25Mbps transmitted signal under conditions of concentrated node loading. These communication failures are eliminated when nodes are used in a distributed configuration. For this reason, it is essential to follow a simple topology rule when using TP/XF-1250 control modules and/or TPT/XF-1250 transceivers and/or TPM-1250 SMX transceivers to eliminate the possibility of reflection-related transmission failures. **No such topology rule applies to the use of TP/XF-78 control modules, TPT/XF-78 transceivers, or TPM-78 SMX transceivers.**

Referred to as the "8-in-16" topology rule, this rule requires that no more than 8 TP/XF-1250 Control Modules and/or TP/XF-1250 Transceivers and/or TPM-1250 SMX Transceivers be located within any 16 meter length of cable. This means that no matter where along the bus the 16 meter measurement is taken, there should be no more than 8 nodes. Figure 7 provides a diagram of such a measurement technique.

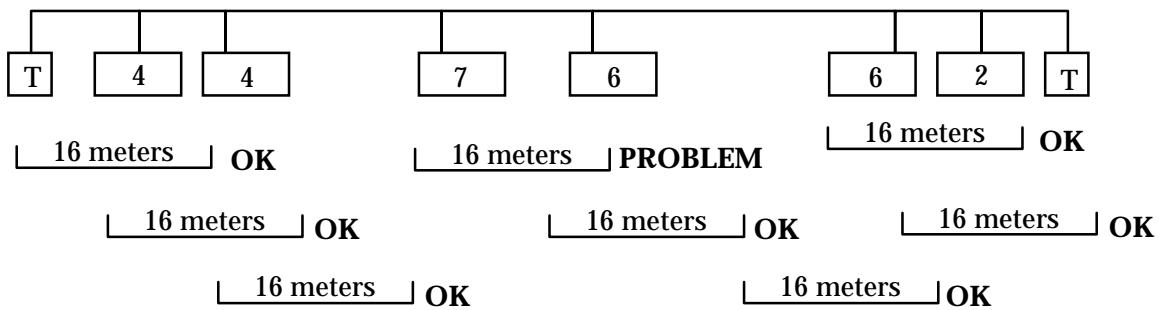


Figure 7 8-in-16 Topology Rule Example

In the example we see an installation with six groups of nodes, varying in size from 2 to 8 devices, in a doubly terminated bus. By using a 16 meter measurement stick that we can move from side-to-side over the length of the bus, we can determine whether the 8-in-16 rule has been met (designated by the word "OK") or violated (shown by the designation "PROBLEM"). In the case of the PROBLEM area, a total of 13 nodes are located within a 16 meter length of the bus, which amounts to five more nodes than are permitted under the 8-in-16 rule.

There are two solutions that can be applied to situations in which the 8-in-16 rule has been, or must be, violated by virtue of the installation scenario. The first and simplest remedy is to insert a router and two termination networks in the bus to break the network into two channels (figure 8). Since each side of the router comprises a different channel, the bus is effectively split and the nodes divided between two channels.

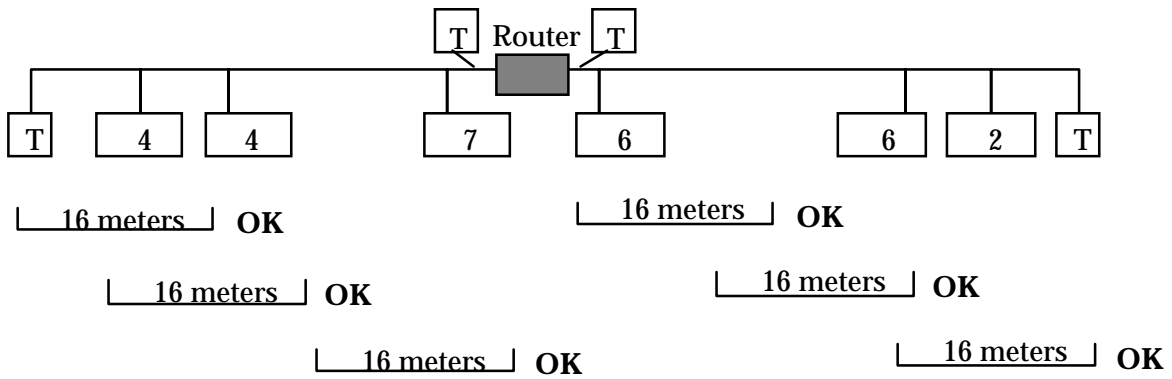


Figure 8 Using a Router to Meet the 8-in-16 Topology Rule

The second remedy to a violation of the 8-in-16 rule is to add additional cable to the bus such that the rule is no longer violated (figure 9). It is important to ensure that the maximum bus length (130 meters of 22AWG/0.65mm Level IV twisted pair) is not exceeded by the additional cable. Due to the complex interactions between the bus and the transceivers with regard to reflections and transmission line delays, it is not possible to substitute an LC network in lieu of the additional cable to resolve this rule violation.

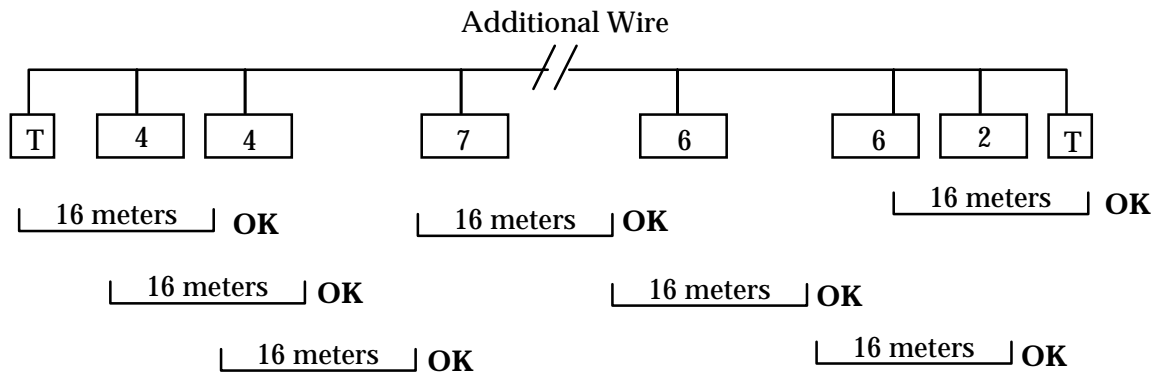
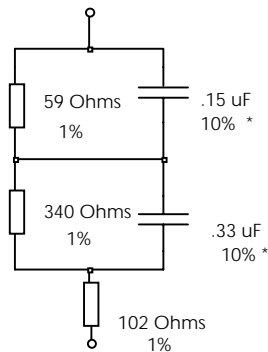


Figure 9 Using Additional Bus Cable to Meet the 8-in-16 Topology Rule

Cable Terminations - TP/XF-78, -1250 Segments

Twisted pair network segments require termination for proper data transmission performance. For doubly terminated bus topologies, a termination must reside at both endpoints of the bus. The terminations required for TP/XF-78, TP/XF-78F, and TP/XF-1250 segments are shown in figure 5.5.



* Capacitors are metal polyester, 50V

Figure 5.5 Required Bus Termination for TP/XF-78 and TP/XF-1250 Twisted Pair Networks

Cable Termination - TP-RS485 Segment

TP-RS485 twisted pair network segments are wired in a doubly terminated bus topology, and a termination must reside at both endpoints of the bus. The termination network shown in Figure 5.5 may be used to terminate a TP-RS485 segment. Alternately, each end of a TP-RS485 segment can be terminated with a 120 Ohm, 5% resistor (a total of two resistors, one at each end of the bus).

RS-485 Grounding

Proper operation of the transmit and receive circuits requires the presence of a signal return path between the circuit grounds of the equipment at each end of the interconnection. The circuit reference may be established by a third conductor connecting the common leads of devices, or it may be provided by connections in each to an earth reference. Where the circuit reference is provided by a third conductor, the connection between circuit common and the third conductor must contain some resistance (i.e., 100 Ohms) to limit circulating current when other ground connections are provided for safety (see Reference [14]).

Chapter 6

Design Issues

This chapter looks at design issues. There is a discussion of Electromagnetic Interference (EMI), and Electrostatic Discharge (ESD), and Designing for Interoperability.

EMI Design Issues

The high-speed digital signals associated with microcontroller designs can generate unintentional Electromagnetic Interference (EMI). High-speed voltage changes generate RF currents that can cause radiation from a product if a length of wire or piece of metal can serve as an antenna.

Products that use the Twisted Pair Control Modules will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the FCC⁵ requires that unintentional radiators comply with Part 15 level “A” for industrial products, and level “B” for products that can be used in residential environments. Similar regulations are imposed in most countries throughout the world^{6,7}.

Echelon has designed the Twisted Pair Control Modules with low enough RF noise levels for design into level “B” products. Echelon encourages level “B” compliance for all LONWORKS-compatible products. This section describes design considerations for control module-based products to meet EMI regulations.

Designing Systems for EMC (Electromagnetic Compatibility)

Echelon has demonstrated that designs using the control modules can meet both FCC and EN55022 level “B” limits. Careful design of application electronics is important to guarantee that a control module-based node will achieve the desired EMC. Information on designing products for EMC is available in several forms including books,⁸ seminars, and consulting services. This section provides useful design tips for EMC. The TP/FT-10 and TP/FT-10F Control Modules have been designed to comply with IEC 801-2, 3, 4 and 5 standards. For more information, see the *FTT-10 Free Topology Transceiver User's Guide* or *FTT-10A Free Topology Transceiver User's Guide*, as applicable.

EMC Design Tips

- Most of the RF noise originates in the CPU portion of the control module, and in any high-frequency or high-speed application circuitry in the node.
- Most of the EMI will be radiated by the network cable and the power cable.
- Filtering is generally necessary to keep RF noise from getting out on the power cable.
- EMI "Keepout" area restrictions should be observed to prevent internal RF noise from coupling onto the network cable.
- The control module must be well grounded within the node to ensure that its built-in EMI filtering works properly.
- Early EMI testing of prototypes at a certified outdoor range is an extremely important step in the design of level “B” products. This testing ensures that grounding and enclosure design questions are addressed early enough to avoid most last-minute changes (and their associated schedule delays).

It is possible for a plastic enclosure to be used with Twisted Pair Control Modules in level “B” applications in some specialized configurations. Since external cables must be kept away from the “RF hot” keepout area on the modules (figure 11), the product configuration must somehow constrain the routing of cables so that they cannot pass across the surface of the plastic enclosure

near the module. During FCC EMI testing, cable position is typically varied to generate maximum emission levels (within constraints of normal product usage).

The three standoff holes on the control module are generally not needed for mechanical support, but the hole nearest connector P2 is important for EMI grounding of the control module. Best results are achieved by a solid ground connection from the control module to the application mother board and to a metalized enclosure using the P2 standoff.

The Twisted Pair Control Modules include adequate filtering on the network data communication lines for most node designs to meet level “B” emission limits. In rare cases, such as designs including circuits with extremely fast edges, additional noise attenuation is required. In such cases it may be necessary to use a common-mode choke, such as muRata’s PLT1R53C connected in series with the data communication lines adjacent to the node’s external network connector. This choke will provide an additional 10dB-to-15dB of EMI attenuation over the 30MHz-to-500MHz range. The choke adds a few pF of differential capacitance to the data communication lines, and therefore reduces network performance and may affect interoperability. In general, application designs should not require a common-mode choke.

Control Module Keepout Areas

Figure 11 shows three “keepout” areas on the control modules. Area one, the “EMI Radiated Keepout Area,” covers the Neuron Chip and the PROM. This is the area of the control module that generates the most RF noise. Cables, long metal chassis parts, and drive circuits for external cables must be kept away from this part of the control module.

Area two, the “EMI Susceptibility Area,” is the main twisted pair transceiver area on the control module, and any RF energy that couples into this part of the module circuit will be conducted out onto the network cable. High frequency and high-speed circuits should be kept well away from this area of the control module (and away from the network connector).

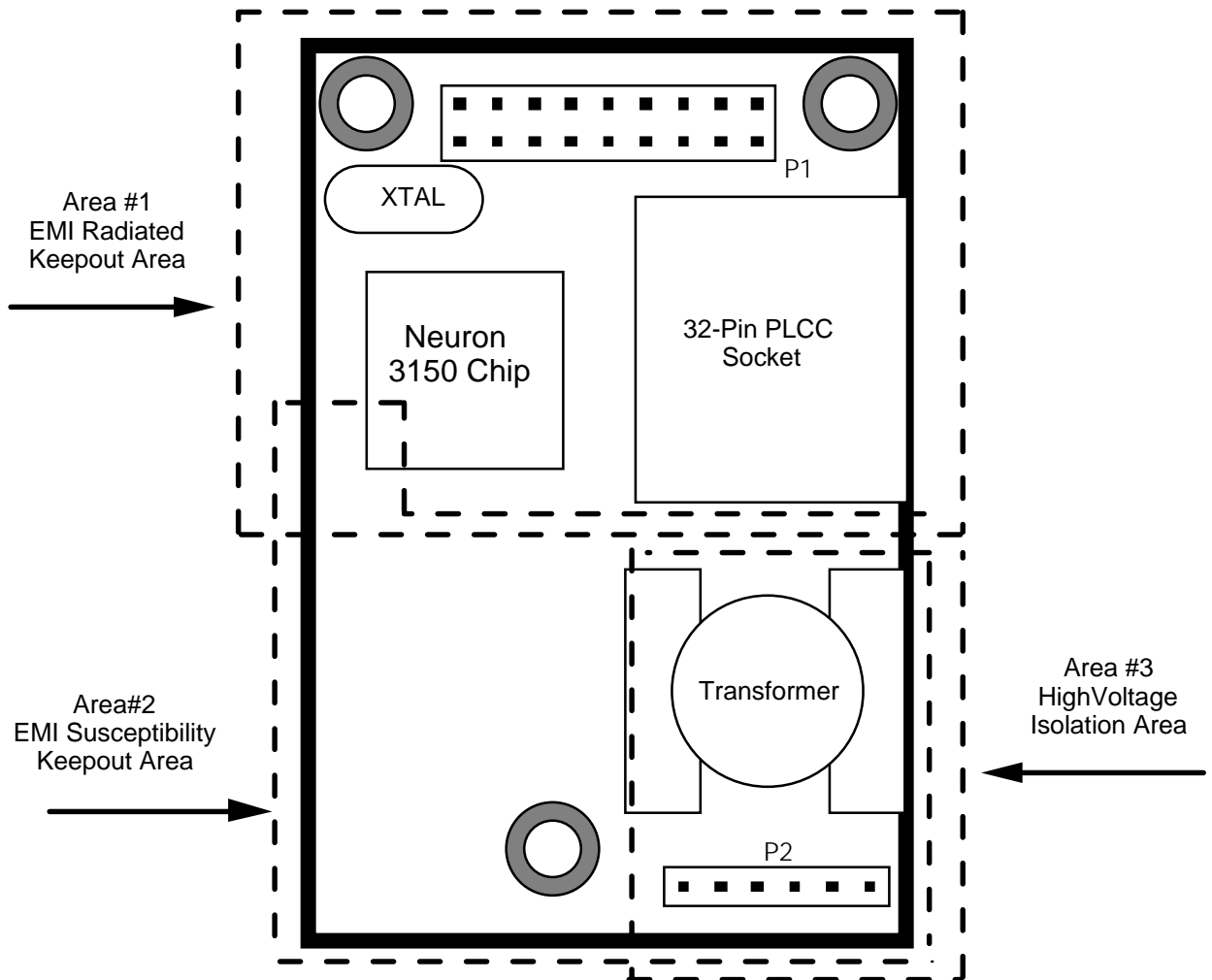


Figure 11 Control Module Keepout Areas

Area three is the “High Voltage Isolation Area.” The transceiver coupling transformer on all control modules (except the TP-RS485) provides electrical isolation between the control module’s local ground (primary side) and the network wiring (secondary side). The transformers and associated filter components are designed to withstand moderately large primary-to-secondary voltages (see the control module data sheets for the exact ratings). To take advantage of this isolation, it is important to keep application circuitry, logic ground, metal chassis parts, and other primary-side components at least 3.8mm (0.15 inches) away from the secondary area on the control module and the network connector.

ESD Design Issues

Electrostatic Discharge (ESD) is encountered frequently in industrial and commercial use of electronic systems⁹. Reliable system designs must consider the effects of ESD and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. The static voltages generated by humans can easily exceed 10kV. Keyboards, connectors, and enclosures provide paths for static discharges to reach ESD sensitive components such as the Neuron Chip. This section describes techniques to design ESD immunity into control module-based products.

Designing Systems for ESD Immunity

ESD hardening includes the following techniques:

- Provide adequate creepage and clearance distances to prevent ESD hits from reaching sensitive circuitry;
- Provide low impedance paths for ESD hits to ground;
- Use diode clamps or transient voltage suppression devices for accessible, sensitive circuits

The best protection from ESD damage is circuit inaccessibility. If all circuit components are positioned away from package seams, the static discharges can be prevented from reaching ESD sensitive components. There are two measures of "distance" to consider for inaccessibility: creepage and clearance. Creepage is the shortest distance between two points along the contours of a surface. Clearance is the shortest distance between two points through the air. An ESD hit generally arcs farther along a surface than it will when passing straight through the air. For example, a 20 kV discharge will arc about 10 mm (0.4 inches) through dry air, but the same discharge can travel over 20mm (0.8 inches) along a clean surface. Dirty surfaces can allow arcing over even longer creepage distances.

When ESD hits to circuitry cannot be avoided through creepage, clearance and ground guarding techniques, i.e., at external connector pins, explicit clamping of the exposed lines is required to shunt the ESD current. Consult Standler⁹ for advice about ESD and transient protection for exposed circuit lines. In general, exposed lines require diode clamps to the power supply rails or zener clamps to chassis ground in order to shunt the ESD current to ground while clamping the voltage low enough to prevent circuit damage. The Neuron Chip's I/O and control lines are connected directly to P1 without any ESD protection beyond that provided by the Neuron Chip itself. If these lines will be exposed to ESD in an application, protection must be added on the application electronics board. Figure 12 shows an example of the use of diode clamps to protect the control module I/O lines in a keypad scanning application.

The TP control modules use diode clamping and transformer isolation to shunt ESD from the network connector P2 to ground. It is therefore important to provide a low impedance ground path from the mounting hole near P2 to the main system ground. The TP/FT-10 also includes spark gaps (designed to arc at approximately 1000 -2000V) between each of the network lines to ground and a diode/capacitor protection circuit to absorb ESD energy. The TP/FT-10F uses similar, but not identical, protection circuitry.

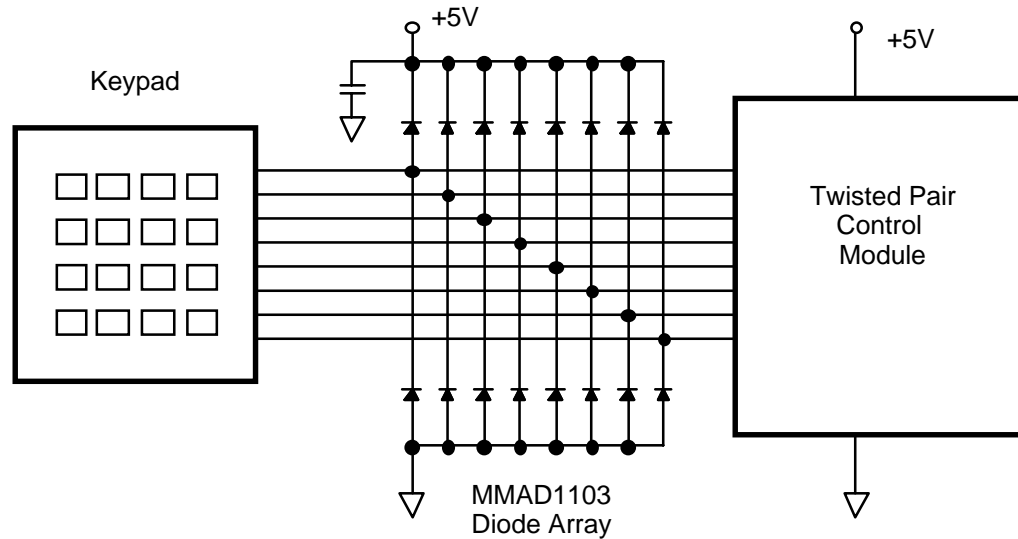


Figure 12 Example of Diode Clamping Protection for Control Module I/O Lines

Designing for Interoperability

In order to meet the LONWORKS interoperability guidelines regarding TP/XF-78, TP/XF-78F, and TP/XF-1250 nodes, the following printed circuit layout guideline for the application electronics board is recommended.

Mutual capacitance of data pair conductors (differential capacitance) from the twisted pair medium tap connector to the connector which mates to the TP/XF control module P2 header must be kept within the maximum limit specified in the table below:

Module type	Maximum mutual capacitance	Maximum PCB trace lengths
TP/XF-78, -78F	5 pF	50 mm
TP/XF-1250	2 pF	20 mm

Chapter 7

Programming Considerations

This section explains the integration of control modules using the LonBuilder Developer's Workbench and NodeBuilder Development tool. It covers considerations relating to memory specifications, device definition, channel definition, and target emulation hardware.

Memory Considerations

The developer must supply a 32 pin PLCC packaged memory device for the exported application image. The TP/XF-78, TP/FT-10, TP/XF-1250, and TP-RS485 modules support read-only access to external memory. The access time requirement for the memory device depends on the control module. The standard TP/XF-78, TP/FT-10, and TP-RS485 Control Modules have a 5MHz input clock and require a memory access time of 200ns or faster. The TP/XF-1250 Control Module has a 10MHz input clock and requires a memory access time of 90 or 120ns or faster depending on the production date of the module. TP/XF-1250 modules produced on or before January, 1995, (revision code A to G) require a 90ns access time or faster. TP/XF-1250 modules produced on or after February 1, 1995, (revision code H or higher) require a 120ns access time or faster. Table 8 shows the vendor part numbers for 32 Kbyte, PLCC OTP ROMs that fit the socket on the control module. Please note that LCC devices that support UV erasures are not physically compatible with the PLCC socket. Atmel AT29C256 devices will work as ROM memory in the control modules designed to use ROMs. Note, however, that none of the PROM-based control modules support write control of the flash memory. Also note that this memory device is not pin compatible with the AT29C257 used in the flash memory-based control modules.

The TP/FT-10F and TP/XF-78F Flash Control Modules have a 10MHz input clock and require an Atmel AT29C257-90J (32K), AT29C517-90J (64K total, 56K usable, 8K unusable), or AT29C010A-90J (128K total, 56K usable, 72K unusable) flash memory with $t_{DS} \leq 35ns$.

The Neuron Chip firmware must be aware of the flash memory sector size to properly support write operations. The AT29C257 has a 64 byte sector size while the AT29C512, and AT29C010A devices have a 128 byte sector size. Using the large memory devices as an alternate part for the AT29C256 requires the generation of a new exported image built with a device definition which contains the correct sector size.

Warning: When programming flash memory, the part must be explicitly secured with Software Data Protection (SDP) enabled by the PROM programmer. If this feature is not supported by the PROM programmer, the program memory may become corrupted.

Emulation Technology, Inc. sells an adapter (part number ET 322801K600-YAM) to support programming PLCC devices using standard 600 mil DIP PROM programmers.

Table 8 Memory Devices

Supplier	90 ns Access time	150-200 ns Access time	Flash Memory
AMD	AM27C256-90JC	AM27C256-200JC	
Atmel	AT29C256-20JC (Flash memory used in read-only applications. Useful during development.)	AT27C256R-20JC	AT29C257-90JC (32K x 8) AT29C512-90JC (64K x 8, 56K usable) AT29C010A-90JC (128K x 8, 56K usable)
Catalyst Semi. Inc.	CAT27HC256N-90		
Intel Corp.		N27C256-200V10	
Microchip Tech.	27HC256-90/L	27C256-20/L	
National Semi.		NMC27C256-20	
Signetics Corp.		27C256-20A	
Silicon Storage Technology			NH29EE512-90 (64K x 8, 56K usable) NH29EE010-90 (128K x 8, 56K usable)
Texas Instruments		TMS27C256-20	

Application Program Development and Export

Application programs are initially developed, tested, and debugged using the LonBuilder Developer's Workbench or the NodeBuilder Development tool. See the *LonBuilder User's Guide* and *NodeBuilder User's Guide* for detailed instructions on developing and testing applications. Refer to the section below which applies to your development platform.

LonBuilder Developer's Workbench

The process of creating programs for the twisted pair control modules requires attention to two main elements of a LonBuilder project definition. These elements include both the Channel definition and Hardware Property definition, and are considered in the following sections.

Channel Definition

Channel setup requires consideration of both hardware and software issues. For software configuration, the LonBuilder tool configures the Neuron Chip communications port according to the channel definition accessed by selecting the *Network* and *Channel* buttons in the LonBuilder Navigator. Create a channel definition to use the *Std Xcvr Type* which matches the control module you wish to target. Always set the option *Enforce Std Type* to *Yes* unless you are making a decision to create devices which are not interoperable. For devices that do not need to meet the LONMARK interoperability guidelines, parameters associated with the number of priority slots, minimum clock rate, and oscillator accuracy may be adjusted for specific applications, but all other parameters must remain unchanged. With the exception of the TP-

RS485 module, the communications rate parameter must not be altered. It is also important to note the control modules do not support collision detection.

The TP/FT-10 channel has special requirements associated with devices which communicate with more than one physical layer repeater in the transmission path. These issues are discussed in both FTT-10 and FTT-10A user's guides^{15,16}.

The hardware associated with the physical connection of the LonBuilder hardware to the targeted twisted pair media is an important development time consideration which includes several options. Table 9 lists the options available for connecting LonBuilder processor cards to the twisted pair network.

Table 9 LonBuilder Twisted Pair Transceiver Options

Control Module	LonBuilder Transceiver Model	Notes
TP/FT-10, TP/FT-10F	Model 77040 FTM-10 Standard Modular Transceiver (SMX ^a) mounted on a Model 27100 LonBuilder SMX Adapter.	Installation requires attention to termination, and processor clock speed options on the 77040.
TP/XF-78, TP/XF-78F	Model 77010 TPM/XF-78 SMX Transceiver mounted on a Model 27100 LonBuilder SMX Adapter, OR a model number 27400 LonBuilder twisted pair transceiver.	The 27400 has been replaced by SMX transceivers. When using an existing 27400 transceiver, verify that both jumper groups are in the TP-78 position.
TP/XF-1250	Model 77030 TPM/XF-1250 SMX Transceiver mounted on a Model 27100 LonBuilder SMX Adapter, OR a model number 27400 LonBuilder twisted pair transceiver.	The 27400 has been replaced by SMX transceivers. When using an existing 27400 transceiver, verify that both jumper groups are in the TP-1250 position.
TP-RS485	Model 77030 TPM/RS485 SMX Transceiver mounted on a Model 27100 LonBuilder SMX Adapter.	

Refer to the *LonBuilder Hardware Guide*¹⁸ and *LONWORKS SMX Transceiver Installation Instructions*¹⁷ for detailed instructions on installing the SMX adapter and the above listed SMX transceivers.

Warning: It is important to set the backplane transceiver jumpers on the LonBuilder processor card to the *External Transceiver* setting prior to installing the SMX adapter.

One common LonBuilder configuration includes a LonBuilder Router (Echelon Model number 75400) which connects the LonBuilder backplane channel to the desired twisted pair media using one of the LonBuilder twisted pair transceivers described in table 9.

When changing the LonBuilder hardware configuration to attach a LonBuilder router to an external twisted pair channel, ensure that the following steps are completed.

- 1** Select a backplane channel for side A and the desired twisted pair channel for side B in the LonBuilder Router `Target HW` definition.
- 2** Ensure that channel A of the router is connected to the backplane channel. For level 1 and 2 routers, a backplane transceiver must be installed in the router P2 channel A transceiver expansion connector. For level 3 routers, JP1 *must* be in the "B" position.
- 3** Mount a compatible LonBuilder twisted pair transceiver on the side "B" expansion connector. For level 3 routers, JP2 *must* be in the "A" position.
- 4** Create a router `Target HW` and `Node Spec` for the LonBuilder Router. In all cases, the `Clock Rate` field for the `Target HW` definition must be 10MHz.
- 5** Use the LonBuilder tool to install and load/start the router.

A heavily loaded twisted pair channel may generate more traffic than can be forwarded through the LonBuilder Router. This may cause the LonBuilder Protocol Analyzer to miss some of the packets on the channel. To prevent lost packets, attach the protocol analyzer directly to the twisted pair channel. This requires an additional transceiver as listed in table 9. When changing the LonBuilder hardware configuration to attach the protocol analyzer to the twisted pair channel, ensure that the following steps are completed.

- 1** Select the desired twisted pair channel in the protocol analyzer `Target HW` definition.
- 2** Mount a compatible LonBuilder twisted pair transceiver on the control processor's P3 expansion connector. For level 3 control processors, JP1 *must* be in the "A" position.
- 3** Use the LonBuilder software to install the protocol analyzer.

The backplane network in the LonBuilder Development Station can approximate the performance of various twisted pair media supported by the control modules. This is accomplished with the following steps.

- 1** For the channel definition, select: Std Xcvr Type: DC-1250.
- 2** Set the Enforce Std Type? option to: 'No'.
- 3** Adjust the values shown to match Bit Rate, Minimum Clock Rate, Average Packet Size, Collision Detect, and Oscillator Accuracy for the targeted standard transceiver.

Hardware Properties

LonBuilder Emulators assigned hardware properties defined with the values shown in tables 10 and 11 will emulate the functional operation and real time performance of a control module.

Table 10 LonBuilder Application Node HW Properties for Each Control Module

Property	TP/FT-10	TP/XF-78	TP-RS485
Neuron Chip	3150	3150	3150
Input Clock	5MHz	5MHz	5MHz
Memory Type	EEPROM	EEPROM	EEPROM
ROM Size (in 256 byte pages)	128 ¹	128 ¹	128 ¹
ROM Start	0	0	0
EEPROM Size	0	0	0
RAM Size	0	0	0
I/O Size	0	0	0

Notes:

1. Use 64 pages to force small applications to run from the Neuron 3150 Chip EEPROM memory.

Table 11 LonBuilder Application Node HW Properties

Property	TP/FT-10F	TP/XF-78F	TP/XF-1250
Neuron Chip	3150	3150	3150
Input Clock	10MHz	10MHz	10MHz
Memory Type	FLASH	FLASH	EEPROM
ROM Size (in 256 byte pages)	0	0	128 ¹
ROM Start	0	0	0
Flash Size	128 for 32Kx8 224 for > 32Kx8	128 for 32Kx8 224 for > 32Kx8	
Flash Start	0	0	
Flash Sector Size ²	64 for 32Kx8 128 for 32Kx8	64 for 32Kx8 128 for 32Kx8	
RAM Size	0	0	0
I/O Size	0	0	0

Notes:

1. Use 64 pages to force small applications to run from the Neuron 3150 Chip EEPROM memory.
2. The sector size is determined by the device selected. Use a 64 byte sector size for AT29C257, and a 128 byte sector size for AT29C512 or AT29C010 devices. The sector size affects the image generated for the flash part. If you specify an AT29C512 as an alternate part for an application that fits in an AT29C257, you **MUST** generate a flash image that is designed to use 128 byte sectors.

An application is initially run on the LonBuilder emulator using the LonBuilder Application Interface Kit, Model 27810, to connect the emulator's I/O signals to the application hardware. If possible, use the LonBuilder to supply power to the application hardware. If this is not possible, you must exercise care when sequencing power to avoid damage to the emulator. Always apply power to the LonBuilder before powering the application hardware. See *MAI Considerations* in Appendix B for more information.

Once the application program is developed and debugged on an emulator, the application is exported from the LonBuilder Developer's Workbench for subsequent programming of a PROM or flash memory device. Again, refer to the *LonBuilder User's Guide* for detailed instructions on how to do this. Before exporting the application, be sure to change the HW Type in the Target Hardware window to Custom. Also verify that the Channel Definition matches the transceiver

type of the targeted control module. Verify the `Channel Definition (Hardware Properties)` before doing a `Build` and final `Export` of the image. Improperly specifying properties is a common mistake that causes Custom Nodes to appear non-functional.

The final application image is generated as a two step process.

- 1 Select the `Project.Build All` command in the `Project` menu to compile and link the application for the custom node being developed; and
- 2 Select the `Export` button in the application node `Node Specs` window. PROMs are programmed using a Neuron ROM image (`.NRI` extension). Flash memory is initially programmed using the Neuron EEPROM/Flash image (`.NEI` extension).

Warning: When programming flash memory, the part must be explicitly secured with Software Data Protection (SDP) enabled by the PROM programmer. If this feature is not supported by the PROM programmer, the program memory may become corrupted.

NodeBuilder Development Tool

Please refer to the *NodeBuilder User's Guide* for detailed instructions on how to develop nodes.

The NodeBuilder software requires specific information about the target control module to create ROM or flash application memory images. Although the definition procedures are somewhat different, the same information is needed for LonBuilder and NodeBuilder tools.

The twisted pair control modules use Echelon standard transceivers. As shipped, the NodeBuilder software makes available standard transceiver definitions for the TP/XF-78, TP/XF-1250, and TP/FT-10 twisted pair channels. Definitions for the TP-RS485 channel may not be visible without modifying the file `NODEBLDR.INI` found in the `C:\WINDOWS` directory. The following line must be included under the `[Interface Options]` section of this file:

```
Show RS485=1
```

The NodeBuilder software uses device template files to represent target device hardware configuration information. Tables 12 and 13 show the values required for the twisted pair control modules for each tab dialog box in the NodeBuilder device template editor. Included with NodeBuilder are template files for some of the control modules. Where possible, the names for existing template files are referenced in tables 12 and 13. Device templates must be created using the NodeBuilder device template editor for modules which are not already defined.

The NodeBuilder LTM-10 provides the initial execution platform for the application under development. Programs are initially developed using the `LTMRAM.DTM` device template to support download and test operations. This execution platform does not support control of the Neuron Chip input clock. The LTM-10 has a 10MHz input clock. Applications targeting twisted pair control modules using a 5MHz input clock must be written to tolerate the reduced execution performance. Connect the LTM-10 to the target I/O circuit using the cable detailed in figure 13 and Echelon Model 21860 Module Application Interface (MAI). The cable and MAI are included with the NodeBuilder Development Tool. The cable also may be easily constructed with common 28 AWG (7x36 stranded) flat ribbon cable and IDC socket connectors on 0.100" (2,54mm) centers. Check that JP1 of the MAI is shunted. See *MAI Considerations* in Appendix B for more information.

Warning: Power application I/O circuits using only one power source. Echelon's plug-in power supply will provide up to 150mA @ 5VDC for the application I/O circuit. Should more power be required, use a suitably regulated 5VDC power supply connected to J4 of the LTM-10 mother board. It is also possible to power the LTM-10 using the application I/O power supply. Avoid using multiple power supplies whenever possible.

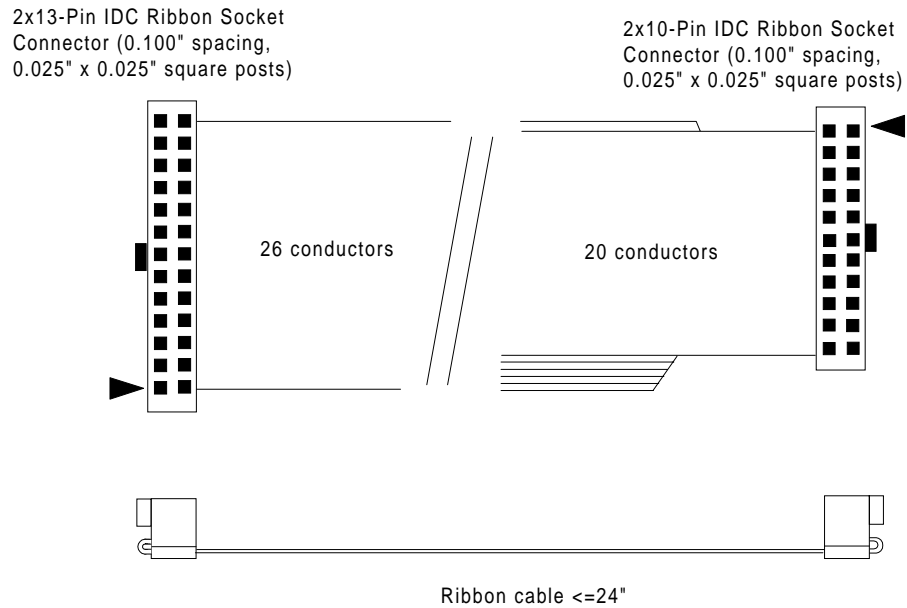


Figure 13 Model 10800 NodeBuilder/Application Interface Cable Detail

Table 12 NodeBuilder Device Template Values for Twisted Pair Control Modules.

	TP/FT-10	TP/XF-78	TP-RS485
NodeBuilder Template File	TPFT10.DTM	TPXF78.DTM	
Hardware			
Target Hardware:	Other	Other	Other
Neuron Model	3150	3150	3150
Clock Speed	5MHz	5MHz	5MHz
Transceiver Type	TP/FT-10	TP/XF-78	TP/RS485-39 ¹ TP/RS485-78 TP/RS485-625
Firmware			
System Image:	Default	Default	Default
Version: ²	-	-	-
Image Name:	SYS3150	SYS3150	SYS3150
Memory Map			
ROM (256 byte Pages): ³	128 (0 - 0x7FFF)	128 (0 - 0x7FFF)	128 (0 - 0x7FFF)
NV RAM:	0	0	0
RAM:	0	0	0
I/O:	0	0	0
Memory Type:	EEPROM	EEPROM	EEPROM

Notes:

1. LONMARK interoperable RS-485 channel.
2. Determined by NodeBuilder when System Image field is set to default. To select a specific version, the System Image field must be set to 'Other Standard Version'.
3. Use 64 pages to force small applications to run from the Neuron Chip 3150 EEPROM memory.

Table 13 NodeBuilder Device Template Values for Twisted Pair Control Modules

	TP/FT-10F	TP/XF-78F	TP/XF-1250
NodeBuilder Template File			TPXF1250.DTM
Hardware			
Target Hardware:	Other	Other	Other
Neuron Model	3150	3150	3150
Clock Speed	10MHz	10MHz	10MHz
Transceiver Type	TP/FT-10	TP/XF-78	TP/XF-1250
Firmware			
System Image:	Default	Default	Default
Version: ¹	-	-	-
Image Name:	SYS3150	SYS3150	SYS3150
Memory Map			
ROM (256 byte Pages): ²	0	0	128 (0 - 0x7FFF)
Flash:	128 for 32Kx8 (0 - 0x7FFF) 224 for > 32Kx8 (0 - 0xDFFF)	128 for 32Kx8 (0 - 0x7FFF) 224 for > 32Kx8 (0 - 0xDFFF)	0
RAM:	0	0	0
I/O:	0	0	0
Memory Type:	Flash	Flash	EEPROM
Flash sector size:	64 for 32Kx8 128 for > 32Kx8	64 for 32Kx8 128 for > 32Kx8	

Notes:

1. Determined by the NodeBuilder software when System Image field is set to default. To select a specific version, the System Image field must be set to 'Other Standard Version'.
2. Use 64 pages to force small applications to run from the Neuron Chip 3150 EEPROM memory.

Programming

The NodeBuilder software generates application image files automatically with each build. Chapter 5 of the *NodeBuilder User's Guide* describes the various data files exported. Once a build is successfully completed using the correct device template file, the next step is to commit the program image to the program memory device using a PROM programmer. The program images generated by the NodeBuilder software are stored in the device directory, with a base file name which matches the device name. ROM/PROM based devices are programmed using the Neuron ROM image file (<device name>.NRI), and the flash based control modules are initially programmed using the Neuron EEPROM/Flash image file (<device name>.NEI).

Warning: When programming flash memory, the part must be explicitly secured with Software Data Protection (SDP) enabled by the PROM programmer. If this feature is not supported by the PROM programmer, the program memory may become corrupted.

8

References

This section provides a list of the reference material used in the preparation of this manual.

Reference Documentation

- [1] *Neuron Chip Data Book* as published by Motorola or Toshiba.
- [2] *LONWORKS Custom Node Development Engineering Bulletin*, Echelon Corporation.
- [3] *LONWORKS TPT Twisted Pair Transceiver Module User's Guide*, by Echelon Corporation.
- [4] *NodeBuilder User's Guide*, by Echelon Corporation.
- [5] 47CFR15, Subpart B (Unintentional Radiators), *U.S. Code of Federal Regulations*, (formerly known as FCC Part 15, Subpart J).
- [6] *VDE 0871*, Class "B", tested per VFG1046/1984.
- [7] EN55022, new EC EMC Standard.
- [8] *Noise Reduction Techniques in Electronic Systems*, 2nd ed., by Henry W. Ott, John Wiley & Sons, 1988.
- [9] *Protection of Electronic Circuits from Overvoltages*, by Ronald B. Standler, John Wiley & Sons, 1989.
- [10] *Electromagnetic Compatibility (EMC), Part 4: Testing and measurement techniques—Section 2: Electrostatic discharge immunity test*, IEC 1000-4-2, 1995-0.
- [11] *Neuron C Programmer's Guide*, by Echelon Corporation.
- [12] *LonBuilder User's Guide*, by Echelon Corporation.
- [13] *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks*, by Echelon Corporation.
- [14] *EIA RS-485 Standard*, Electronic Industries Association, 1983. This document is available through Global Engineering Documents in Irvine, California at +1-714-261-1455 or 1-800-854-7179.
- [15] *LONWORKS FTT-10 Free Topology Transceiver User's Guide*, by Echelon Corporation.
- [16] *LONWORKS FTT-10A Free Topology Transceiver User's Guide*, by Echelon Corporation.
- [17] *LONWORKS SMX Transceiver Installation Instructions*, by Echelon Corporation.
- [18] *LonBuilder Hardware Guide*, by Echelon Corporation.

Appendix A

Application I/O Development Considerations

This appendix provides hints and suggestions to aid developers of application I/O hardware targeted for the Twisted Pair Control Modules. The I/O circuit designer is constrained by the programming model and internal hardware of the Neuron Chip. The constraints on I/O pin usage are defined in Reference [1].

State Transition Timing

The state transition timing for Neuron Chip I/O signals after reset depends on the external memory included in the node implementation. The control modules contain a fixed set of memory resources which do not include external RAM. Therefore, the I/O state transitions during reset are bounded by the slowest input clock frequency, 5MHz. Figure 14 shows typical I/O state transition behavior for a 5 MHz module during reset. The TP/FT-10F, TP/XF-78F, and TP/XF-1250 modules running at 10MHz will take roughly 61ms to achieve the initial I/O pin state after the rising edge of the reset signal.

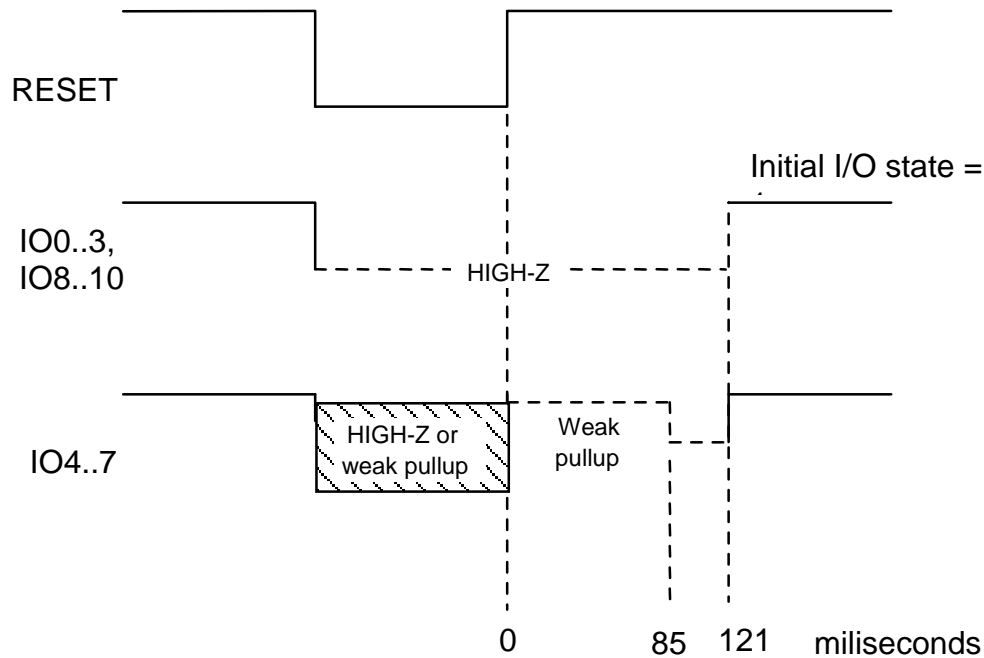


Figure 14 Output Pin State Transitions for 5MHz Control Modules

MAI Considerations

The LonBuilder and NodeBuilder tools include a Model 21860 Module Application Interface (MAI) and cable that can be used in place of a twisted pair control module for testing your target device. The cable connects the MAI to a LonBuilder Application Interface Board or a NodeBuilder LTM-10 Node.

The MAI has two jumpers to control the power distribution for the I/O circuit under development. If JP1 is installed, the I/O circuit under development can use up to 400 mA of regulated +5V from the LonBuilder processor board or NodeBuilder LTM-10 Node through the pin P1.12. If JP2 is installed, 35 mA of regulated +12V from the LonBuilder processor board is available through pin P1.1 (+12V is not available on the LTM-10 node). If the power supply circuit for the target device sources the power, JP1 and JP2 must be removed.

The AIB does not buffer the 11-I/O and ~SERVICE pins of the Neuron Chip. The ~SERVICE signal only reaches the interface adapter if the JP4 jumper marked on the AIB is installed.

The ~RESET signal on the AIB is a buffered CMOS input to the Neuron Chip on the Emulator. This buffering does not allow direct testing of an I/O circuit using ~RESET as an output from the Neuron Chip.

