The FT 5000 Smart Transceiver is our next-generation chip for smart networks. It is the key product in the LonWorks® 2.0 platform—the next generation of LonWorks products designed to greatly increase the power and capability of LONWORKS enabled devices, while lowering development and node costs.

The FT 5000 Smart Transceiver integrates a high-performance Neuron® Core with a free topology twisted-pair transceiver. Combined with the new low-cost FT-X3 Communications Transformer and inexpensive serial memory, the FT 5000 Smart Transceiver provides a lower-cost, higher-performance LONWORKS solution than previous-generation FT Smart Transceivers.

**Features**

- 3.3V operation.
- Higher-performance Neuron® Core —internal system clock scales up to 80MHz.
- Substantial device price reduction.
- Serial memory interface for inexpensive external EEPROM and flash non-volatile memories.
- Supports up to 254 Network Variables (NVs) and 127 aliases.
- Low-cost surface mount FT-X3 Communications Transformer.
- User-programmable interrupts provide faster response time to external events.
- Includes hardware UART with 16-byte receive and transmit FIFOs.
- 7 mm x 7 mm 48-pin QFN package.
- Supports polarity-insensitive free topology star, daisy chain, bus, loop, or mixed topology wiring.

www.echelon.com
• Compliant with TP/FT-10 channels using FT 3120®/FT 3150® Smart Transceivers and FTT-10/FTT-10A/LPT-10/LPT-11 Transceivers.
• 12 I/O pins with 35 programmable standard I/O models.
• Supports up to 42KB of application code space.
• 64KB RAM (44KB user-accessible) and 16KB ROM on-chip memories.
• Unique 48-bit Neuron ID in every device for network installation and management.
• Very high common-mode noise immunity.
• -40°C to +85°C operating temperature range.

Description

The FT 5000 Smart Transceiver includes three independent 8-bit logical processors to manage the physical MAC layer, the network, and the user application. These are called the Media-Access Control (MAC) processor, the network (NET) processor, and the application (APP) processor, respectively (see Figure 1). At higher system clock rates, there is also a fourth processor to handle interrupts.

The FT 5000 Smart Transceiver supports Polarity-insensitive cabling using a star, bus, daisy-chain, loop, or combination topology (see Figure 2). Thus, installers don’t have to follow a strict set of wiring rules imposed by other networking technologies. Instead, they can install wiring in the fastest and most cost-effective manner, thereby saving time and money. Free topology wiring also simplifies network expansion by eliminating restrictions on wire routing, splicing, and device placement.

Enhanced Performance

Faster system clock. The internal system clock for the FT 5000 Smart Transceiver can be user-configured to run from 5MHz to 80MHz. The required external crystal provides a 10MHz clock frequency, and an internal PLL boosts the frequency to a maximum of 80MHz as the internal system clock speed. The previous-generation Neuron 3120/3150 Core divided the external oscillator frequency by two to create the internal system clock. An FT 5000 Smart Transceiver running with an 80MHz internal system clock is thus 16 times faster than a 10MHz Neuron 3120/3150 Core running.

The 5MHz internal system clock mode in the FT 5000 Smart Transceiver provides backward compatibility to support timing-critical applications designed for the 10MHz FT 3150 or FT 3120 Smart Transceiver.

The Neuron Core inside the FT 5000 Smart Transceiver includes a built-in hardware multiplier and divider to increase the performance of arithmetic operations.

Backward Compatibility

The FT 5000 Smart Transceiver is fully compliant with the TP/FT-10 channel and can communicate with devices that use Echelon’s FTT-10/FTT-10A Transceivers, FT 3120/FT 3150 Smart Transceivers, or LPT-10/LPT-11 Link Power Transceivers.

The Neuron Core in the FT 5000 Smart Transceiver uses the same instruction set and architecture as the previous-generation Neuron Core, with two new additional instructions for hardware multiplication and division. The Series 5000 Neuron Core is source code compatible with applications written for the Series 3100 Neuron Core. Applications written for the Series 3100 Neuron Core must be recompiled with the NodeBuilder® FX Development Tool or the Mini FX Evaluation Kit before they can be used with the FT 5000 Smart Transceiver.

The FT 5000 Smart Transceiver uses Neuron firmware version 19. Firmware versions prior to version 19 are not compatible with the FT 5000 Smart Transceiver. The Neuron firmware is pre-programmed into the on-chip ROM. The FT 5000 Smart Transceiver can also be configured to read newer firmware from external memories, allowing the firmware to be upgraded over time.

Support for more network variables.

Because it uses Neuron firmware version 19, the FT 5000 Smart Transceiver supports applications with up to 254 network variables and 127 aliases for Neuron hosted devices (devices without a host microprocessor). A Series 3100 Neuron Chip or Smart Transceiver with Neuron firmware version 15 or earlier supports up to 62 network variables and 62 aliases for Neuron hosted devices. Series 3100 chips with Neuron firmware version 16 or later support up to 254 network variables. You must use the NodeBuilder FX Development Tool to take advantage of 254 network variables.

Interrupts. The FT 5000 Smart Transceiver lets developers define application interrupts to handle asynchronous events triggered by selected state changes on any of the 12 I/O pins, by on-chip hardware timer-counter units, or by an on-chip high-performance hardware system timer. An application uses the Neuron C interrupt() clause to define the interrupt condition and the interrupt task that handles the condition. The Neuron C program runs the interrupt task.
whenever the interrupt condition is met. See the Neuron C Programmer’s Guide for more information about writing interrupt tasks and handling interrupts.

**JTAG.** The FT 5000 Smart Transceiver provides an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG) to allow a Series 5000 chip to be included in the boundary-scan chain for device production tests. A Boundary Scan Description Language (BSDL) file for the FT 5000 Smart Transceiver can be downloaded from Echelon’s Web site.

**I/O Pins and Counters**
The FT 5000 Smart Transceiver provides 12 bidirectional I/O pins that are 5V-tolerant and can be configured to operate in one or more of 35 predefined standard input/output models. The chip also has two 16-bit timer/counters that reduce the need for external logic and software development.

**Memory Architecture**
The FT 5000 Smart Transceiver uses inexpensive external serial EEPROM and flash memories for non-volatile application and data storage, and optionally for future Neuron firmware upgrades. It has 16KB of ROM and 64KB (44KB user-accessible) of RAM on the chip. It has no on-chip non-volatile memory (EEPROM or flash) for application use. Each chip, however, contains its unique Neuron identifier (Neuron ID) in an on-chip, non-volatile, read-only memory.

The application code and configuration data are stored in the external non-volatile memory (NVM) and copied into the internal RAM during device reset; the instructions then execute from internal RAM. Writes to NVM are shadowed in the internal RAM and pushed out to external NVM by the Neuron firmware (see Figure 2). The application does not manage NVM directly.

**External memories supported.** The FT 5000 Smart Transceiver supports two serial interfaces for accessing off-chip, non-volatile memories: serial Interface (I2C) and serial peripheral interface (SPI). EEPROM and flash memory devices can use either the I2C interface or the SPI interface. However, at the time of publication, there are no serial flash parts that use the I2C protocol and meet the required specifications for the Series 5000 external memory interface.

External serial EEPROMs and flash devices, which are inexpensive and come in very small form factors, are available from multiple vendors.

The FT 5000 Smart Transceiver requires at least 2KB of off-chip memory available in an EEPROM device to store the configuration data. The application code can be stored either in the EEPROM (by using a larger-capacity EEPROM device) or in a flash memory device used in addition to the 2KB minimum EEPROM. Thus, the external memory for the FT 5000 Smart Transceiver has one of the configurations listed in Table 1:

<table>
<thead>
<tr>
<th>Configuration</th>
<th>EEPROM</th>
<th>SPI</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I2C</td>
<td></td>
<td>A single I2C EEPROM memory device, from 2KB to 64KB in size.</td>
</tr>
<tr>
<td>2</td>
<td>I2C</td>
<td>SPI</td>
<td>One I2C EEPROM (at least 2KB in size) and a single SPI EEPROM memory device.</td>
</tr>
<tr>
<td>3</td>
<td>SPI</td>
<td></td>
<td>A single SPI EEPROM memory device, from 2KB to 64KB in size.</td>
</tr>
<tr>
<td>4</td>
<td>SPI</td>
<td></td>
<td>One SPI EEPROM (at least 2KB in size, up to 64KB in size, but the system uses only the first 2KB of the EEPROM memory).</td>
</tr>
</tbody>
</table>

Table 1: Allowed External Memory Device Configurations

As Table 1 shows, the FT 5000 Smart Transceiver supports using a single EEPROM memory device, or a single EEPROM memory device plus a single flash memory device.

If the FT 5000 Smart Transceiver detects an external flash memory device, the flash memory represents the entire user non-volatile memory for the device. That is, any additional EEPROM memory beyond the mandatory 2KB is not used.

**Using the I2C Interface.** When using the I2C interface for external EEPROM, the FT 5000 Smart Transceiver is always the master I2C device (see Figure 3). The clock speed supported for the I2C serial memory interface is 400kHz (fast I2C mode). The I2C memory device must specify I2C address 0. Both 1-byte and 2-byte address modes are supported, but 3-byte addressing mode is not.
the area shadowed from external NVM into the RAM.

- On-chip RAM for stack segments and RAMNEAR data.
- Mandatory external EEPROM that holds configuration data and non-volatile application variables.
- Reserved space for system use.

If a 64KB external serial EEPROM or flash device is used, the maximum allowed size of application code is 42KB as defined by extended NVM area in the memory map. An additional 16KB of the remaining space can hold an external system firmware image, in case a future firmware upgrade is required.

communications transformer (the FT-X3). The transformer enables operation in the presence of high frequency common-mode noise on unshielded twisted-pair networks. Properly designed devices can meet the rigorous Level 3 requirements of EN 61000-4-6 without the need for a network isolation choke. The transformer also offers outstanding immunity from magnetic noise, eliminating the need for protective magnetic shields in most applications.

The FT 5000 Smart Transceiver and the FT-X3 Communications Transformer are designed to be used as a pair, and therefore must be implemented together in all designs. No transformer other than the FT-X3 (or FT-X1 or FT-X2) communications transformer may be used with the FT 5000 Smart Transceiver or the smart transceiver warranty will be void.

Migration Considerations

Most device designs that use the previous-generation FT 3120/3150 Smart Transceiver can transition to the FT 5000 Smart Transceiver. However, because the two generations have different supply voltage and memory architecture, hardware redesign of the boards is required to transition to the FT 5000 Smart Transceiver.

See the Series 5000 Chip Data Book for more information about migrating device designs for FT 3120/3150 Smart Transceivers to the FT 5000 Smart Transceiver.

End-to-End Solutions

A typical FT 5000 Smart Transceiver-based device requires a power source, crystal, external memory, and an I/O interface to the device being controlled (see Figure 7 for a typical FT 5000 Smart Transceiver-based device).

Noise Immunity

A LonWorks device based on the FT 5000 Smart Transceiver is composed of two components: the FT 5000 Smart Transceiver and an external communications transformer (the FT-X3). The transformer enables operation in the presence of high frequency common-mode noise on unshielded twisted-pair networks. Properly designed devices can meet the rigorous Level 3 requirements of EN 61000-4-6 without the need for a network isolation choke. The transformer also offers outstanding immunity from magnetic noise, eliminating the need for protective magnetic shields in most applications.

Figure 8: FT 5000 Smart Transceiver Pin Configuration

FT 5000 Smart Transceiver
IC Pin Descriptions

All digital inputs are low-voltage transistor-transistor logic (LVTTL) compatible, low leakage, 5V-tolerant. All digital outputs are slew-rate limited to reduce Electromagnetic Interference (EMI).

### Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SVC~</td>
<td>1</td>
<td>Digital I/O</td>
<td>Service (active low)</td>
</tr>
<tr>
<td>I00</td>
<td>2</td>
<td>Digital I/O</td>
<td>100 for I/O Objects</td>
</tr>
<tr>
<td>I01</td>
<td>3</td>
<td>Digital I/O</td>
<td>101 for I/O Objects</td>
</tr>
<tr>
<td>I02</td>
<td>4</td>
<td>Digital I/O</td>
<td>102 for I/O Objects</td>
</tr>
<tr>
<td>I03</td>
<td>5</td>
<td>Digital I/O</td>
<td>103 for I/O Objects</td>
</tr>
<tr>
<td>VDD1V8</td>
<td>6</td>
<td>Power</td>
<td>1.8 V Power Input (from internal voltage regulator)</td>
</tr>
<tr>
<td>I04</td>
<td>7</td>
<td>Digital I/O</td>
<td>104 for I/O Objects</td>
</tr>
<tr>
<td>VDD3V3</td>
<td>8</td>
<td>Power</td>
<td>3.3 V Power</td>
</tr>
<tr>
<td>I05</td>
<td>9</td>
<td>Digital I/O</td>
<td>105 for I/O Objects</td>
</tr>
<tr>
<td>I06</td>
<td>10</td>
<td>Digital I/O</td>
<td>106 for I/O Objects</td>
</tr>
<tr>
<td>I07</td>
<td>11</td>
<td>Digital I/O</td>
<td>107 for I/O Objects</td>
</tr>
<tr>
<td>I08</td>
<td>12</td>
<td>Digital I/O</td>
<td>108 for I/O Objects</td>
</tr>
<tr>
<td>I09</td>
<td>13</td>
<td>Digital I/O</td>
<td>109 for I/O Objects</td>
</tr>
</tbody>
</table>
### FT 5000 Smart Transceiver Pin Description

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO10</td>
<td>14</td>
<td>Digital I/O</td>
<td>IO10 for I/O Objects</td>
</tr>
<tr>
<td>IO11</td>
<td>15</td>
<td>Digital I/O</td>
<td>IO11 for I/O Objects</td>
</tr>
<tr>
<td>VDDV8</td>
<td>16</td>
<td>Power</td>
<td>1.8 V Power Input (from internal voltage regulator)</td>
</tr>
<tr>
<td>TRST~</td>
<td>17</td>
<td>Digital Input</td>
<td>JTAG Test Reset (active low)</td>
</tr>
<tr>
<td>VDD3V3</td>
<td>18</td>
<td>Power</td>
<td>3.3 V Power</td>
</tr>
<tr>
<td>TCK</td>
<td>19</td>
<td>Digital Input</td>
<td>JTAG Test Clock</td>
</tr>
<tr>
<td>TMS</td>
<td>20</td>
<td>Digital Input</td>
<td>JTAG Test Mode Select</td>
</tr>
<tr>
<td>TDI</td>
<td>21</td>
<td>Digital Input</td>
<td>JTAG Test Data In</td>
</tr>
<tr>
<td>TDO</td>
<td>22</td>
<td>Digital Output</td>
<td>JTAG Test Data Out</td>
</tr>
<tr>
<td>XIN</td>
<td>23</td>
<td>Oscillator Input</td>
<td>Crystal oscillator Input</td>
</tr>
<tr>
<td>XOUT</td>
<td>24</td>
<td>Oscillator Output</td>
<td>Crystal oscillator Output</td>
</tr>
<tr>
<td>VDDPLL</td>
<td>25</td>
<td>Power</td>
<td>1.8 V Power Input (from internal voltage regulator)</td>
</tr>
<tr>
<td>GNDPLL</td>
<td>26</td>
<td>Power</td>
<td>Ground</td>
</tr>
<tr>
<td>VOUTV8</td>
<td>27</td>
<td>Power</td>
<td>1.8 V Power Output (of internal voltage regulator)</td>
</tr>
<tr>
<td>RST~</td>
<td>28</td>
<td>Digital I/O</td>
<td>Reset (active low)</td>
</tr>
<tr>
<td>VIN3V3</td>
<td>29</td>
<td>Power</td>
<td>3.3 V input to internal voltage regulator</td>
</tr>
<tr>
<td>VDD3V3</td>
<td>30</td>
<td>Power</td>
<td>3.3 V Power</td>
</tr>
<tr>
<td>AVDD3V3</td>
<td>31</td>
<td>Power</td>
<td>3.3 V Power</td>
</tr>
<tr>
<td>NETN</td>
<td>32</td>
<td>Communications</td>
<td>Network Port (polarity insensitive)</td>
</tr>
<tr>
<td>AGND</td>
<td>33</td>
<td>Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>NETP</td>
<td>34</td>
<td>Communications</td>
<td>Network Port (polarity insensitive)</td>
</tr>
<tr>
<td>NC</td>
<td>35</td>
<td>N/A</td>
<td>Do Not Connect</td>
</tr>
<tr>
<td>GND</td>
<td>36</td>
<td>Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>TXON</td>
<td>37</td>
<td>Digital I/O</td>
<td>TxActive for optional network activity LED</td>
</tr>
<tr>
<td>RXON</td>
<td>38</td>
<td>Digital I/O</td>
<td>RxActive for optional network activity LED</td>
</tr>
<tr>
<td>CP4</td>
<td>39</td>
<td>N/A</td>
<td>Connect to V&lt;sub&gt;DD3&lt;/sub&gt; through a 4.99 kΩ pullup resistor</td>
</tr>
</tbody>
</table>

### Electrical Characteristics

#### FT 5000 Smart Transceiver Operating Conditions

<table>
<thead>
<tr>
<th>Parameter&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DD3&lt;/sub&gt;</td>
<td>Supply voltage</td>
<td>3.00 V</td>
<td>3.3 V</td>
<td>3.60 V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Low-voltage indicator trip point</td>
<td>2.70 V</td>
<td>2.96 V</td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;s&lt;/sub&gt;</td>
<td>Ambient temperature</td>
<td>-40°C</td>
<td>+85°C</td>
<td></td>
</tr>
<tr>
<td>f&lt;sub&gt;XIN&lt;/sub&gt;</td>
<td>XIN clock frequency&lt;sup&gt;2&lt;/sup&gt;</td>
<td>-</td>
<td>10.000 MHz</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Digital Pin Characteristics

The digital I/O pins (IO0–IO11) have LVTTL-level inputs. Pins IO0–IO7 also have low-level-detect latches. The RST- and SVC- pins have internal pull-ups, and the RST- pin has hysteresis.

Table 4 below lists the characteristics of the digital I/O pins, which include IO0–IO11 and the other digital pins listed in Table 2.

**Table 3: FT 5000 Smart Transceiver Operating Conditions**

**Notes**
1. All parameters assume nominal supply voltage (V<sub>DD3</sub> = 3.3 V ± 0.3 V) and operating temperature (T<sub>o</sub> between -40°C and +85°C), unless otherwise noted.
2. See Clock Requirements in the Series 5000 Chip Data Book for more detailed information about the XIN clock frequency.
3. Assumes no load on digital I/O pins, and that the I/O lines are not switching.
4. Current consumption in Transmit mode represents a peak value rather than a continuous usage value because a Series 5000 device does not typically transmit data continuously.

**Table 4: FT 5000 Smart Transceiver Pin Description**

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS0~</td>
<td>40</td>
<td>Digital I/O</td>
<td>SPI slave select 0 (CS0~, active low) (for external memory connection only)</td>
</tr>
<tr>
<td>VDD3V3</td>
<td>41</td>
<td>Power</td>
<td>3.3 V Power</td>
</tr>
<tr>
<td>VDD3V3</td>
<td>42</td>
<td>Power</td>
<td>3.3 V Power</td>
</tr>
<tr>
<td>SDA_CSR1</td>
<td>43</td>
<td>Digital I/O</td>
<td>SPI serial data (SDA) SPI: slave select 1 (CS1~, active low) (for external memory connection only)</td>
</tr>
<tr>
<td>VDDV8</td>
<td>44</td>
<td>Power</td>
<td>1.8 V Power Input (from internal voltage regulator)</td>
</tr>
<tr>
<td>SCL</td>
<td>45</td>
<td>Digital I/O</td>
<td>PC serial clock (SCL) (for external memory connection only)</td>
</tr>
<tr>
<td>MOSI</td>
<td>46</td>
<td>Digital I/O</td>
<td>SPI master output, slave output (MISO) (for external memory connection only)</td>
</tr>
<tr>
<td>SCK</td>
<td>47</td>
<td>Digital I/O</td>
<td>SPI serial clock (SCK) (for external memory connection only)</td>
</tr>
<tr>
<td>PAD</td>
<td>49</td>
<td>Ground Pad</td>
<td>Ground</td>
</tr>
</tbody>
</table>
Table 4: FT 5000 Smart Transceiver

<table>
<thead>
<tr>
<th>Param-&lt;br&gt;eter&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Description</th>
<th>Minimum&lt;sup&gt;2&lt;/sup&gt;</th>
<th>Typical</th>
<th>Maximum&lt;sup&gt;2&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;HYS&lt;/sub&gt;</td>
<td>Input hysteresis for RST- pin</td>
<td>300 mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;N&lt;/sub&gt;</td>
<td>Input leakage current</td>
<td>-</td>
<td>10 µA</td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;Pu&lt;/sub&gt;</td>
<td>Pullup resistance&lt;sup&gt;2&lt;/sup&gt;</td>
<td>13 kΩ</td>
<td>23 kΩ</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;Pu&lt;/sub&gt;</td>
<td>Pullup current when pin at 0 V</td>
<td>130</td>
<td>275 µA</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. All parameters assume nominal supply voltage (V<sub>DD</sub> = 3.3 V ± 0.3 V) and operating temperature (TA between -40ºC and +85ºC), unless otherwise noted.
2. Applies to RST- and SVC- pins only.

Recommended FT 5000 Smart Transceiver Pad Layout

Figure 9: FT 5000 Smart Transceiver Pad Layout

Smart Transceiver IC Mechanical Specification

Notes:
1. All dimensions are in millimeters.
3. Package warpage max. 0.08 mm.
4. Package corners unless otherwise specified are R0.175±0.025 mm.

Table 5: FT-X3 Communications Transformer Pin Assignments

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NETA</td>
<td>4</td>
<td>NETA connection to LonWorks network</td>
</tr>
<tr>
<td>CTP2</td>
<td>5</td>
<td>Center tap primary 2</td>
</tr>
<tr>
<td>NETN</td>
<td>6</td>
<td>NETN connection from FT 5000 Smart Transceiver</td>
</tr>
<tr>
<td>NETB</td>
<td>7</td>
<td>NETB connection to LonWorks network</td>
</tr>
<tr>
<td>CTS1</td>
<td>8</td>
<td>Center tap secondary 1</td>
</tr>
</tbody>
</table>

Figure 10: FT 5000 Smart Transceiver IC Mechanical Specifications

Notes:
1. All dimensions are in millimeters.
3. Package warpage max. 0.08 mm.
4. Package corners unless otherwise specified are R0.175±0.025 mm.

Recommended FT-X3 Communications Transformer Pad Layout

The FT-X3 Communications Transformer is rotationally symmetric. Hence, the transformer package does not have a marking for Pin 1.

Figure 11: FT-X3 Communications Transformer Pinout Diagram

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NETP</td>
<td>1</td>
<td>NETP connection from FT 5000 Smart Transceiver</td>
</tr>
<tr>
<td>CTP1</td>
<td>2</td>
<td>Center tap primary 1</td>
</tr>
<tr>
<td>CTS2</td>
<td>3</td>
<td>Center tap secondary 2</td>
</tr>
</tbody>
</table>

Figure 12: FT-X3 Communications Transformer Electrical Connection Schematic (winding connections are made on the PCB)

Figure 13: FT-X3 Transformer SMT Layout Pad Pattern
FT 5000 Tape and Reel Information

Devices are uniformly loaded in the carrier tape such that the device pin one is oriented in quadrant 1 toward the side of the tape having round sprocket holes. Figure 15 illustrates the pin-one location.

Recommendation: Add vias to the ends of each pin pad connection (just outside of the SMT pad rectangles) to provide additional mechanical support for the transformer.

FT-X3 Communications Transformer Mechanical Specification

Figure 15: FT 5000 Pin One Orientation

Figure 16 shows the outline dimensions of the carrier tape.

Figure 16: Carrier Tape Outline Drawing

Ao = Bo = 7.25
Ko = 1.10

Notes
1. All dimensions are in millimeters.
2. Tolerances unless noted: 1PL + 0.2, 2PL + 0.1
3. 10 Sprocket hole pitch cumulative tolerance +0.2
4. Camber in compliance with EIA 481.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

For more information, refer to EIA-481-B, Taping of Surface Mount Components for Automatic Placement.

Figure 17 shows the FT 5000 Series 13” Reel Drawing and Specification.
Figure 18 shows the 5000 Series 7” Reel Drawing and Specification.

<table>
<thead>
<tr>
<th>TAPE WIDTH</th>
<th>W1 MAX</th>
<th>W1 MIN</th>
<th>W2 MAX</th>
<th>W2 MIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>8MM</td>
<td>330</td>
<td>100</td>
<td>8.4</td>
<td>14.4</td>
</tr>
<tr>
<td>12MM</td>
<td>330</td>
<td>100</td>
<td>12.4</td>
<td>18.4</td>
</tr>
<tr>
<td>16MM</td>
<td>330</td>
<td>100</td>
<td>16.4</td>
<td>22.4</td>
</tr>
<tr>
<td>24MM</td>
<td>330</td>
<td>100</td>
<td>24.4</td>
<td>30.4</td>
</tr>
<tr>
<td>32MM</td>
<td>330</td>
<td>100</td>
<td>32.4</td>
<td>38.4</td>
</tr>
<tr>
<td>44MM</td>
<td>330</td>
<td>100</td>
<td>44.4</td>
<td>50.4</td>
</tr>
<tr>
<td>56MM</td>
<td>330</td>
<td>100</td>
<td>56.4</td>
<td>62.4</td>
</tr>
</tbody>
</table>

Figure 17: FT 5000 13” Reel and Hub Drawing

Figure 18 shows the 5000 Series 7” Reel Drawing and Specification.

FT-X3 Packing Specifications

Notes
1. All dimensions are in millimeters.
2. Tolerances unless noted: 1PL + ; 2PL + 0.2; 3PL + 0.1; ANG + 0.5°; FRACT +

Figure 19 shows the placement of each device on the carrier tape.

Figure 20 shows the 1.3” Reels/4” Hub.

Notes
1. Material: Black conductive polystyrene PS
2. Inspect per EIA-481-3 standard.
3. Tape thickness: 0.5 ±0.05 mm
4. 10 Sprocket hole pitch cumulative tolerance ±0.20
5. Carrier chamber is within 1 mm in 100 mm
6. Packing length per 22” reel: 10.2 meters
7. Packing length per 13” reel: 3.4 meters
8. Component load per 13” reel: 100 PCS
9. Compression strength: 1.5 kgf min.
10. Environment-Related substance must meet DELTA’s general spec no. 10000-0162
Specifications

Data Communications Type
Differential Manchester encoding.

Network Polarity
Polarity insensitive.

Isolation between Network and FT 5000 IC
0-60Hz, 60 seconds: 1,000V rms; 0-60Hz, continuous: 277V rms.

EMI
Designed to comply with FCC Part 15 Subpart B and EN55022 Level B.

ESD
Designed to comply with EN 61000-4-2, Level 4.

Radiated Electromagnetic Susceptibility
Designed to comply with EN 61000-4-3, Level 3.

Fast Transient/Burst Immunity
Designed to comply with EN 61000-4-4, Level 4.

Surge Immunity
Designed to comply with EN 61000-4-5, Level 3.

Conducted RF Immunity
Designed to comply with EN 61000-4-6, Level 3.

Transmission Speed
78 kilobits per second.

Number of Transceivers per Segment
Up to 64.

Network Wiring
24 to 16 AWG twisted pair; see Series 5000 Chip Data Book or Junction Box and Wiring Guidelines engineering bulletin for qualified cable types.

Network Length in Free Topology
500m (1,640 feet) maximum total wire with no repeaters.
500m (1,640 feet) maximum device-to-device distance.

Network Length in Doubly-terminated Bus Topology
2700m (8,850 feet) with no repeaters.

Maximum Stub Length in Doubly-terminated Bus Topology
3m (9.8 ft)

Network Termination
One terminator in free topology; two terminators in bus topology (more details in Series 5000 Chip Data Book).

Power-down Network Protection
High impedance when unpowered.

Operating Temperature
-40 to 85 °C

Operating Humidity
25-90% RH @ 50 °C, non-condensing (FT-X3 Communications Transformer).

Non-operating Humidity
95% RH @ 50 °C, non-condensing (FT-X3 Communications Transformer).

Vibration
1.5g peak-to-peak, 8Hz-2kHz (FT-X3 Communications Transformer).

Mechanical Shock
100g (peak) (FT-X3 Communications Transformer).

Reflow Soldering Temperature Profile

Peak Reflow Soldering Temperature
260°C (FT 5000 Smart Transceiver).
245°C (FT-X3 Communications Transformer).

Co-planarity
0.12 mm (FT-X3 Communications Transformer).

Mass
6g (FT-X3 Communications Transformer).

Notes
1. Safety agency hazardous voltage barrier requirements are not supported.
2. Network segment length varies, depending on wire type. See Junction Box and Wiring Guidelines engineering bulletin for detailed specifications.

Ordering Information
FT 5000 Smart Transceiver
14235R-2000
14235R-500
FT-X3 Communications Transformer
14255R-100

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